Serial ATA II:

Electrical Specification

Revision 1.0
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Dell Computer Corporation

Intel Corporation

Maxtor Corporation

Seagate Technology

Vitesse Semiconductor Corporation

This 1.0 revision of the Serial ATA II: Electrical Specification ("Final Specification") is available for product design. Product implementations should ensure compliance with this specification.

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For more information about Serial ATA, refer to the Serial ATA Working Group website at www.serialata.org.

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1 Scope

The purpose of this document is to provide a technical specification of a high-speed serialized ATA data link interface. Normative information is provided to allow a technical design team to construct a device that will operate correctly with another device designed to this specification. Informative information is provided to help illustrate the normative material.

2 Goals, objectives and migration considerations

3 Normative references

SATA Specifications (Located on www.serialata.org):
Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a, 7-January-2003
Errata to Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a.
Erratas 42, 47 and 48.
Erratas 50 and 52 [In Work]
Design Guides to Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a. Errata 47
Design Guides 01 through 14, 15B, 16-19
Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.1, 9-October-2003
Serial ATA II: Cable and Connector Specification, Volume 1
Serial ATA II: Cable and Connector Specification, Volume 2 [In Work]

SAS Specification (Located on www.T10.org):
T10/1562-D Information Technology, Serial Attached SCSI (SAS), Revision 5, 9 July 2003

JEDEC Standards (Located on www.jedec.com):
JESD22-A114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
JESD22-C101-A, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components"

4 Definitions, abbreviations, and conventions

5 General overview

6 Physical layer

6.1 Overview

This section describes the physical layer of Serial ATA. The information that is provided is comprised of two types – informative and normative. Unless otherwise described, the information should be considered normative in nature and is included in this document as a necessary requirement in order to properly allow a piece of equipment to attach to another piece of equipment. The normative information is deliberately structured to constrain and define areas only to the degree that is required for compatibility. The information that is provided and marked informative is provided only to help the reader better understand the normative sections and should be taken as examples only. Exact implementations may vary.

This specification is one of a series of specifications that comprise Serial ATA II. This specification includes the Serial ATA 1.0a specification and defines enhancements to that specification that provide additional capabilities while retaining Serial ATA 1.0a compatibility and desktop cost structure. Additional features and capabilities are defined in a way that allow them to be selectively deployed, as business and market conditions require. Capabilities are defined in a way that costs associated with new feature support are incurred if and when the feature is implemented in order to realize customer benefit/value.

Some of the goals and requirements for the specification include:

- Compatibility is maintained with Serial ATA 1.0a
- New features/capabilities is separable/optional proper supersets of Serial ATA 1.0a
- Specifications for 3.0 Gb/s links speeds is provided
- Support for hot pluggable devices in Backplane applications is provided
- Support for system-to-system interconnects is provided
- Where possible, supports interoperability with Serial Attached SCSI (SAS).

6.1.1 Goals

The goal of this specification is to expand upon the Serial ATA 1.0 Electrical Specifications to include specifications for 3.0 Gb/s ("Gen2") speeds. Also, new Electrical Specifications are included to support the targeted applications of Serial ATA II which include backplanes and system-to-system interconnects (see section 6.1.7).

The following terms have been developed for the various Electrical Specifications:

- **Gen1i**: Generation 1 Electrical Specifications: These are the 1.5 Gb/s electrical specifications previously released in Serial ATA 1.0a for PC motherboard to device applications. These specifications are copied here for completeness.
- **Gen1m**: Generation 1 Electrical Specifications for "Short" Backplane and External Desktop Applications: These are the 1.5 Gb/s electrical specifications previously released in "Serial ATA II: Extensions to Serial ATA 1.0" aimed at short 1.5 Gb/s internal backplane applications and the Single-Lane Desktop Cable application. These include only modified Transmitter and Receiver Differential Swing specifications. All other electrical specifications relating to Gen1m compliance points are identical to Gen1i specifications. This specification is for these limited applications only and is not intended for any other system topology.
- **Gen2i**: Generation 2 Electrical Specifications: These are newly developed 3.0 Gb/s electrical specifications, described here, aimed at PC motherboard to device applications.
- **Gen2m**: Generation 2 Electrical Specifications for "Short" Backplane and External Desktop Applications: These are newly defined 3.0 Gb/s electrical specifications aimed only at these applications. These include only modified Transmitter and Receiver Differential Swing specifications. All other electrical specifications relating to Gen2m compliance points are identical to Gen2i specifications. This specification is for this limited application only and is not intended for any other system topology.
- **Gen1x**: Extended Length 1.5 Gb/s Electrical Specification or "Gen1x": These are newly developed electrical specifications, described here, aimed at 1.5 Gb/s links in "long" backplanes and system-to-system applications. These specifications are based upon Serial Attached SCSI Electrical specifications (CT/CR specifications as called out in SAS).
- **Gen2x**: Extended Length 3.0 Gb/s Electrical Specification: These are newly developed electrical specifications, described here, aimed at 3.0 Gb/s links in "long" backplanes and system-to-system applications. These specifications are based upon Serial Attached SCSI Electrical specifications (CT/CR specifications as called out in SAS).

6.1.2 System Specifications

All specifications in this section apply to a Generation 1 and Generation 2 Serial ATA devices.

Table 1: General system specifications

Name	Nom	Units	Description
Φ_{G1}	1.2	Gbits/s	1st Generation 8b data rate
ϕ_{G1}	1.5	Gbits/s	1st Generation 10b bit rate
Φ_{G2}	2.4	Gbits/s	2nd Generation 8b data rate
ϕ_{G2}	3.0	Gbits/s	2nd Generation 10b bit rate
Φ_{G3}	4.8	Gbits/s	3rd Generation 8b data rate
ϕ_{G3}	6.0	Gbits/s	3rd Generation 10b bit rate

6.1.3 List of services

- Transmit a 1.5Gb/sec or 3.0 Gb/sec differential NRZ serial stream at specified voltage levels
- Provide a 100 Ohm matched termination (differential) at the transmitter
- Serialize a 10, 20, 40, or other width parallel input from the Link for transmission
- Receive a 1.5 Gb/sec or 3Gb/s differential NRZ serial stream with data rates of ±350ppm with +0/-5000 ppm (due to SSC profile) from the nominal data rate
- Provide a 100 Ohm matched termination (differential) at the receiver
- Extract data (and, optionally, clock) from the serial stream
- De-serialize the serial stream
- Detect the K28.5 comma character and provide a bit and word aligned 10, 20, 40, or other width parallel output
- Provide specified OOB signal detection and transmission
- Use Out-of-Band Signaling protocol for Initializing the SATA Interface, and use this OOB Burst Signaling sequence to execute a pre-defined Speed Negotiation function.
- Perform proper power-on sequencing and speed negotiation
- Provide device status to Link layer
  - device present
  - device absent
  - device present but failed to negotiate communications
- Optionally support power management modes (note: if not supported, power management requests shall be properly rejected by the Link layer)
- Optionally perform transmitter and receiver impedance calibration (if manufacturing tolerances require)
- Handle the input data rate frequency variation due to a spread spectrum transmitter clock .
- Accommodate request to go into Far-End retimed loopback, and other BIST FIS test modes of operation when commanded (exit this mode on OOB COMRESET/COMINIT)

6.1.4 Goals of Gen2i Electrical Specifications

The Gen2i Electrical Specification aims at the desktop and mobile market for Serial ATA drives. The primary consideration in this application is to maintain complete backwards compatibility with existing Serial ATA 1.0a devices. Secondly, the one meter cable and connectors defined in Serial ATA 1.0a shall operate correctly with both Gen1i and Gen2i devices.

Gen2i is defined with the following goals and requirements:

- Maintains full compatibility with Serial ATA 1.0a
- Defines characteristics of 3.0 Gb/s link.
- Targets only internal cabled configurations using the previously specified 1m cable. No direct connectivity to backplanes or external interfaces.
- Supports lower cost device architectures

6.1.5 Goals of Gen1m/2m Electrical Specifications

The Gen1m/2m Electrical Specifications aim at “Short Backplanes” and External Desktop applications for Serial ATA devices. The primary consideration in this application is to maintain compatibility with Gen1i/2i specifications with the following exceptions. Minimum Transmitter amplitudes are increased and Minimum Receive amplitudes are decreased in order to accommodate additional signal attenuation expected in these applications.

Gen1m/2m are defined with the following goals and requirements:

- Maintains significant compatibility with Serial ATA 1.0a (Gen1i) and Gen2i Electrical Specifications at these newly defined compliance points.
- Defines characteristics of 1.5 (Gen1m) and 3.0 (Gen2m) Gb/s link.
- Targets only “Short Backplane” applications and External Desktop applications.
- All other Electrical Specifications are identical to Gen1i (for Gen1m) or Gen2i (for Gen2m).

The Electrical Specifications are given in section 6.2.

6.1.6 Goals of Gen1x and Gen2x Electrical Specifications

The Gen1x and Gen2x Electrical Specifications aim at the several new Serial ATA II applications which include backplane and system-to-system interconnection. The primary consideration here is to provide robust, hot swappable / hot pluggable interfaces at 1.5 and 3.0 Gb/s.

Gen1x and Gen2x are defined with the following goals and requirements:

- Maintains full compatibility with protocols of Serial ATA 1.0a and Serial ATA II Extensions.
- Defines Electrical Specifications for 1.5 Gb/s (Gen1x) and 3.0 Gb/s (Gen2x) link speeds.
- Targets both backplanes and external interfaces.
- Supports Hot Swappability and Hot Pluggability.
- Aims at compatibility with Serial Attached SCSI (SAS) CT and CR specifications wherever possible as long as impact on cost is not significant.

6.1.7 Targeted Applications

While Serial ATA 1.0a aimed at the interface between desktop PC motherboards, devices, CD-ROMs and DVD-ROMs, the Serial ATA II specification targets a much wider set of applications. This section illustrates some, but not all, of the potential applications for the Serial ATA II interface which take advantage of the new features of Serial ATA II such as switching, queuing and enclosure management.

6.1.7.1 Internal 1 meter Cabled Host to Device

In this application, Gen1i or Gen2i electrical specifications compliant points are located at the Serial ATA mated connectors on both the PC Motherboard and Device. The cable, specified in Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a, January 7, 2003, operates at both 1.5 and 3.0 Gb/s. The application need not comply with Hot Plug Electrical Specifications.

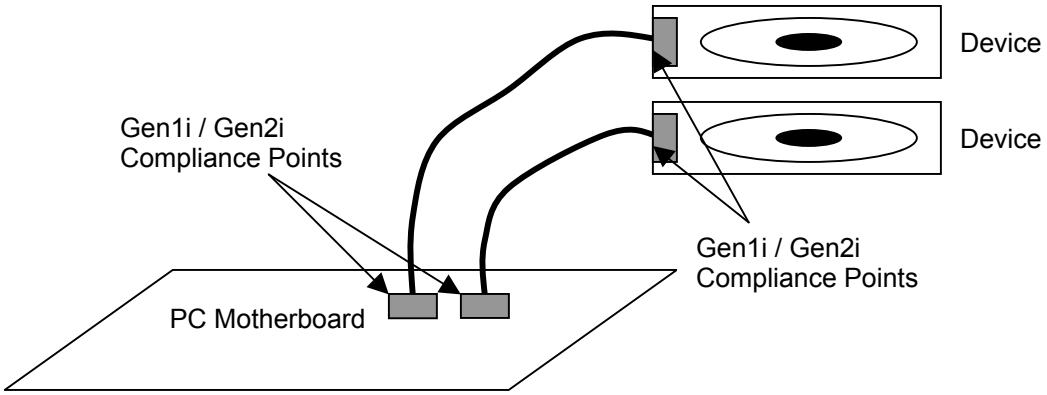


Figure 1: Internal 1 meter Cabled Host to Device Application

6.1.7.2 "Short" Backplane to Device

In this application, Gen1i/2i disk drives within a small disk array are installed into Drive Canisters which are plugged into a "short" backplane. The I/O Controller connecting to the Backplane shall contain a Host component which exceeds Gen1i/2i Transmitter and Receiver Differential Swings specifications so that the signals at the I/O Controller connector complies with the Gen1m/2m electrical specifications. All other electrical specifications at this compliance point shall meet Gen1i/2i specifications. Compliant points are located at the Serial ATA mated connectors on both the device (Gen1i/2i) and the I/O Controller (Gen1m/2m). The application does not contain a cable but routes Serial ATA signals on printed circuit board at 1.5 and 3.0 Gb/s where it is anticipated that the backplanes attenuate signals more than the Serial ATA 1.0a compliant copper cable. The burden falls on the I/O Controller to increase transmit signal swing and accommodate smaller receive swings at the I/O controller connector. The Gen1i/2i drives are not required to comply with the Hot Plug specifications of this document. However, in practical terms, the application benefits from Hot Plug capable compliant devices.

NOTE: At Gen2 speeds the designer faces significant challenges regarding signal integrity issues. Validation/Feasibility data at Gen2 speeds has not been provided. Making this work is up to the system designer.

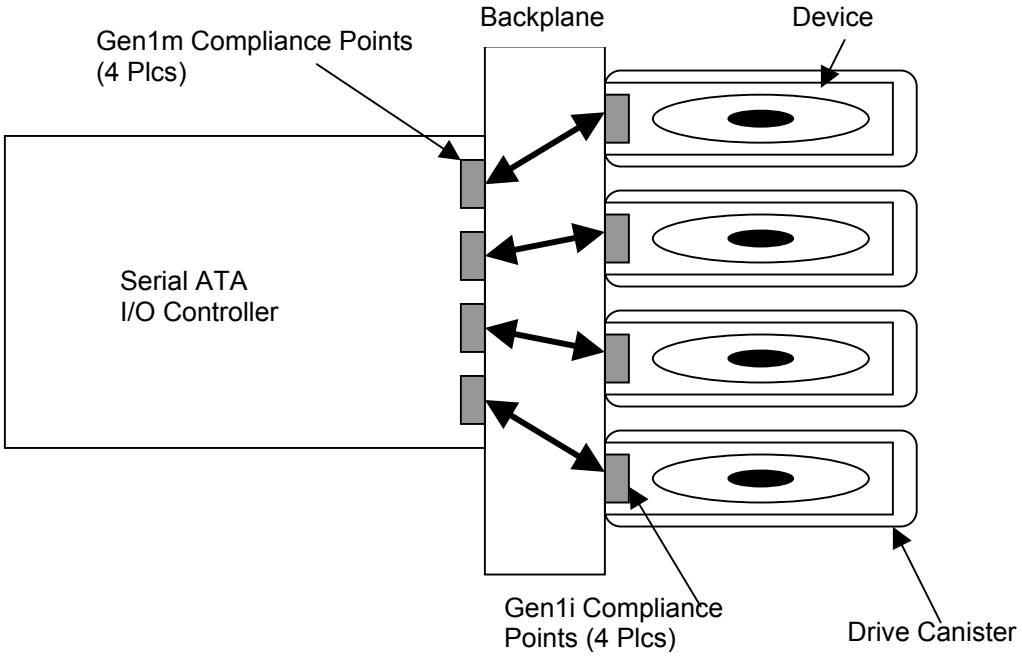


Figure 2: Short Backplane to Device Application

6.1.7.3 “Long” Backplane to Device

In this 1.5 or 3.0 Gb/s application, the length of the backplane is longer than in the previous example so attenuation of signals reduce their amplitude beyond usable levels. Therefore an IC may be placed between the device and the canister’s connector to the backplane to convert the disk’s Gen1i/Gen2i levels to Gen1x/Gen2x levels. A typical circuit might be a Serial ATA Port Selector. Likewise, the I/O Controller complies with Gen1x/Gen2x levels at the backplane connector to the I/O Controller. This allows reliable transmission of Serial ATA data over backplanes longer than in the “Short Backplane” Application described above. The burden of determining whether a Backplane Application is “Short” or “Long” falls upon the system designer who must analyze their system’s attenuation. Compliant points are located at the Serial ATA mated connectors on both the canister (Gen1x/Gen2x) and the I/O Controller (Gen1x/Gen2x). The Gen1x/Gen2x Electrical Specifications require Hot Plug capability so that the disk/canister can be plugged and unplugged without damage.

NOTE: Since Gen1x and Gen2x drive/canister assemblies are interchangeable they shall be interoperable in all applications.

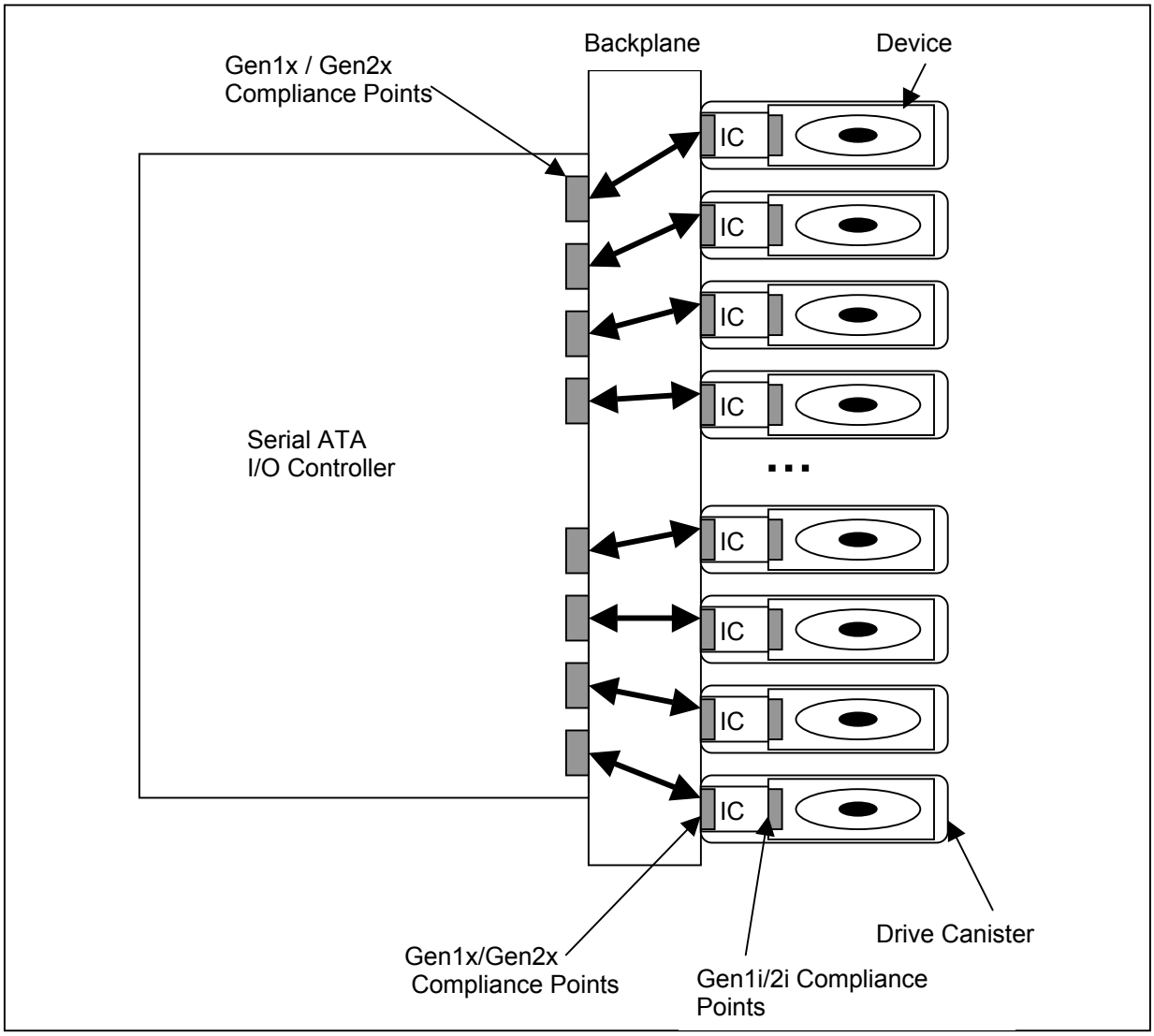


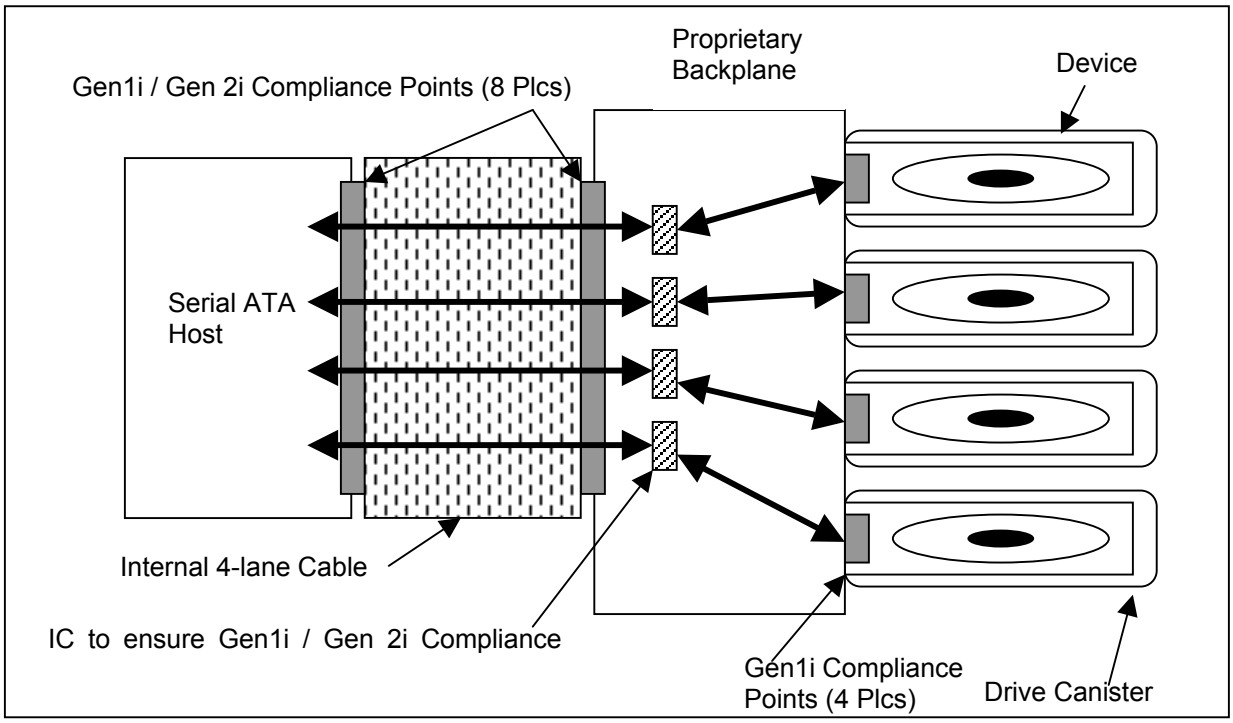
Figure 3: Long Backplane to Device Application

6.1.7.4 Internal 4-lane Cabled Serial ATA Disk Arrays

In this application, Gen1i and Gen2i Serial ATA drives are connected to the host controller via the internal 4-lane cable solution. Gen1i and Gen2i specifications shall be met at each end of the 4-lane cable mated interface. The internal 4-lane cable shall connect to the device by one of the following two approaches.

- The host end of the internal 4-lane solution shall mate directly to the host controller board. The device end shall consist of four individual single lane Serial ATA cables for direct mate with up to four individual Serial ATA devices.
- The host end of the internal 4-lane solution shall mate directly to the host controller board. The device end of the internal 4-lane cable shall consist of a single internal 4-lane connector mated to a backplane which will provide individual connection points to up to four Serial ATA devices. The backplane design is proprietary.

In the second solution, attenuation of the backplane will reduce signal amplitude below specification limits at the compliance points. An IC, such as a Port Selector, shall be placed between the device and the internal 4-lane cable mated interface. Gen1i and Gen2i specifications shall be met at each end of the 4-lane cable mated interface and the device mated connector interface.



NOTE: For Gen2i drives the link from the host to the drive (through the IC on the backplane) does not have an electrical specification for the “delivered signal” to the drive. Consider the compliance point for the backplane-drive connector (through the mated pair). If the signal at the compliance point, into a lab load meets all the requirements of Table 2: General Specifications and Table 4: Transmitted Signal Requirements, and the backplane meets all the requirements of Table 3: Transmitter Specifications, then interoperability is confirmed.

However, it is anticipated that the additional trace length on the backplane between the IC and the backplane-drive connector make compliance to these specifications difficult. Therefore the burden for ensuring interoperability with all Gen1i/2i drives falls upon the implementer of the system. This work falls outside of the capabilities of this document. Essentially the implementer would use simulations and empirical results to confirm that the compliance point at the backplane-drive connector is equivalent to or better than a compliant Host and Cable combination.

6.1.7.5 System to System Interconnects – Data Center Applications

NOTE: This application uses the "External Multi-Lane Cable/Connector" defined in "Serial ATA II: Cable and Connector, Volume 2".

In this application, Gen1x or Gen2x Electrical Specifications are used to connect two systems together using an external cable (defined elsewhere). This differs from the Application described in 6.1.6.5 "External Desktop Application" because this application requires higher quality cables/connectors that meet the longer distance requirements of Data Center Storage applications, albeit at a potentially higher cost. A rule of Serial ATA II is that all external cables will function at both 1.5 and 3.0 Gb/s. Use of a cable that will operate at 1.5 Gb/s but not at 3.0 Gb/s is allowed but this cable assembly shall not be interchangeable with standard Serial ATA cables. For example, if this 1.5 Gb/s cable uses Serial ATA specified connectors, the cable shall be keyed by the user to ensure that it could not plug into standard Serial ATA connections. Hot Pluggability is a requirement in this application. Compliance points are located at the mated bulkhead connectors of each system.
Gen1i, Gen2i and Gen1m specifications are not allowed for these external interfaces.

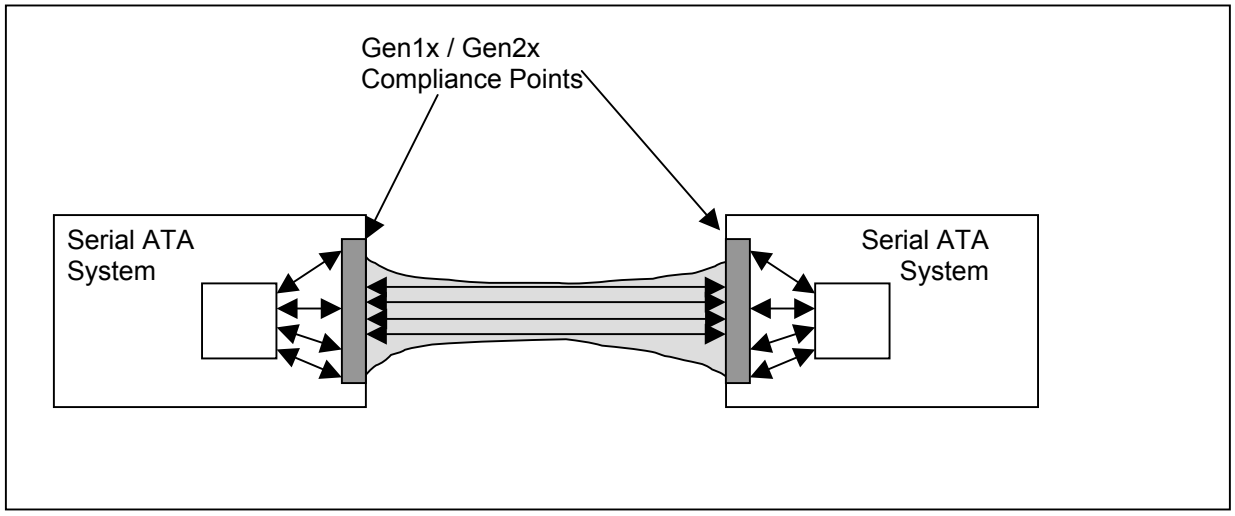


Figure 4: System to System Interconnects

6.1.7.6 System to System Interconnects – External Desktop Applications

NOTE: This application uses the "External Single-Lane Cable/Connector" defined in "Serial ATA II: Cable and Connector, Volume 2".

This application is aimed at cost-sensitive external storage applications that require approximately 2 meters of cable distance but less than the Data Center Application.

In the example shown below, in this application, a Device Enclosure contains a Gen1i / Gen2i device and an interposer card which contains an integrated circuit unless the device is specifically designed for external connection. Regardless of the implementation, the outside of the Device Enclosure shall meet Gen1m specifications when operating at Gen1 speeds and Gen2m specifications when operating at Gen2 speeds. A cable/connector has been defined for this application which operates at both Gen1 and Gen2. The Host System has an external connector which meets Gen1m specifications when operating at Gen1 speeds and Gen2m specifications when operating at Gen2 speeds.

The entire system shall meet the following requirements:

- The cable/connector shall operate at Gen1 and Gen2 speeds. Systems shall not deploy any cable which cannot operate at Gen2 speeds when the Host System and Device Enclosure both comply with Gen2m electrical specifications.
- The Host System and Device Enclosure shall comply with Gen1m specifications when operating at Gen1 speeds.
- The Host System and Device Enclosure may operate at Gen2 speeds. However, if they operate at Gen2 speeds the Host System and Device Enclosure shall comply with Gen2m specifications when operating at Gen2 speeds and shall also be able to operate at Gen1 speeds using Gen1m electrical specifications.
- The Host System and the Device Enclosure shall comply with the Hot Plug Specifications in this document.
- NOTE: AC Coupling on the Transmitters and Receivers of the Serial ATA System and Device Enclosure is strongly recommended for Gen1m and required for Gen2m.

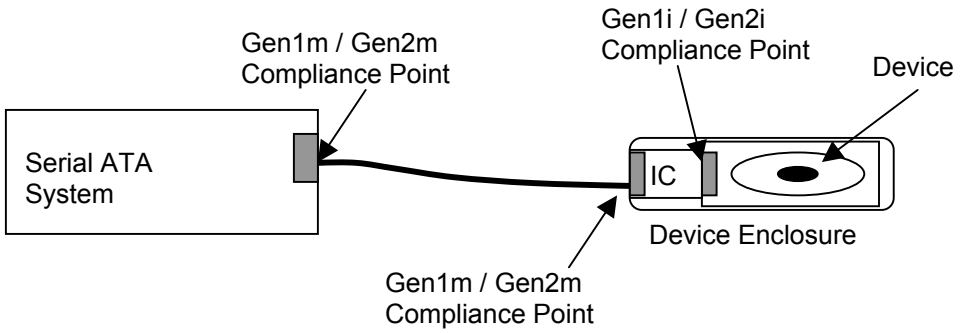


Figure 5: External Desktop Application

6.1.7.7 Proprietary Serial ATA Disk Arrays

In this application, Serial ATA drives are connected to a backplane and the links are routed over a combination of internal backplanes or cables as well as an external cable to a Serial ATA system. There are not semiconductors between the drives and the system so the intermediate connectors are NOT compliance point. Although this application is allowed, the external connectors on the Disk Array must NOT be standard Serial ATA connectors. This is to prevent users from connecting standard external cables between the system and the disk array since they may not function reliably.

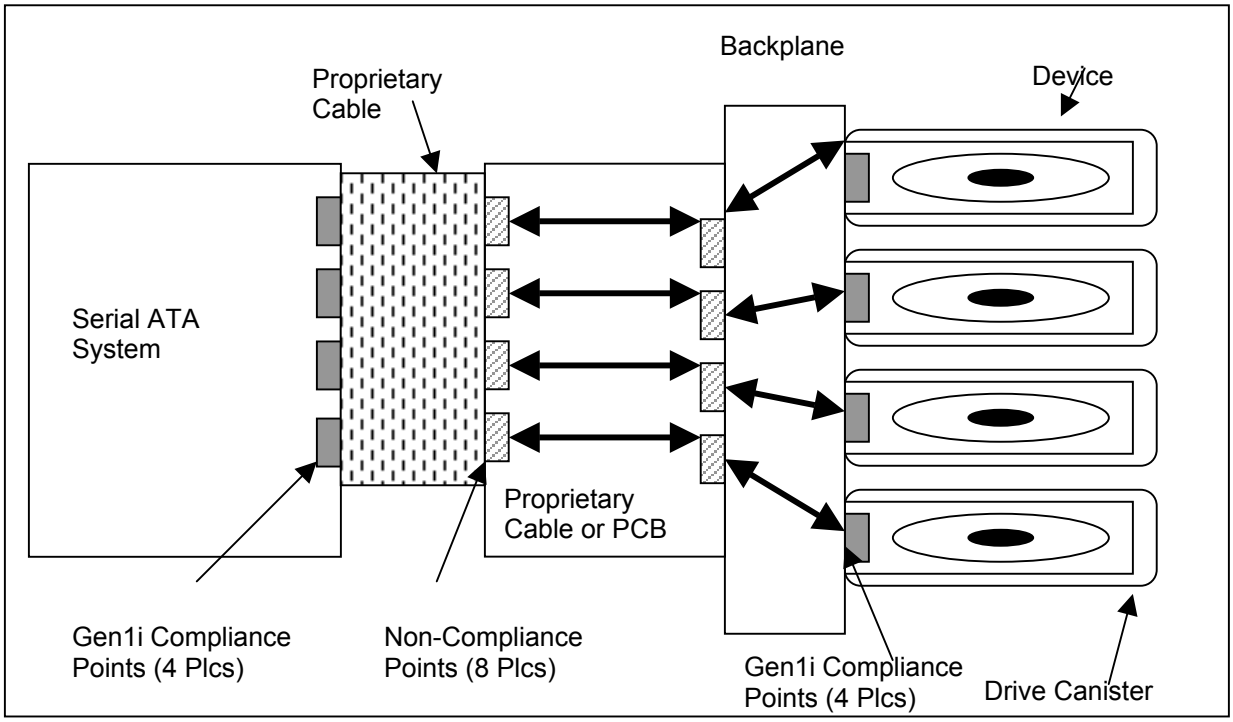


Figure 6: SATA Disk Arrays

6.1.7.8 Serial ATA and SAS

The “T10/1562-D Standard: Information Technology - Serial Attached SCSI (SAS) Specification, Revision 5, 9 July 2003” documents a standard for mapping SCSI protocol across a serial link. The SAS Standard borrows heavily from the SATA PHY, Link, and Transport layers. A SAS domain may, optionally, support attachment to and control of unmodified SATA Devices connected directly into the SAS domain using the Serial ATA Tunneled Protocol (STP).

The SAS dual-port target connector is a superset of the SATA device connector. The connectors are keyed such that a SAS device (called a target device in SAS) cannot be plugged directly into a SATA backplane or SATA cable, but SATA Devices can plug into SAS backplane and cable receptacles. SAS initiator devices use the SATA Host connector, and may use the SATA Cable (Gen1i/2i 1 meter cable from SATA 1.0a specification). Note that in SAS, there is an extra set of signal pins added to support dual-ported SAS target devices. This function is not used in SATA devices. The SAS PHY specifications at this connector (XT/XR) are backwards compatible with SATA devices. This is done in a manner that is transparent to the SATA Device without requiring any modification to the Serial ATA device. Nothing in this specification changes Serial ATA in order to make Hosts or Devices compliant to any SAS Specification.

The only exception to this last statement is that the Gen1x/Gen2x specifications are based upon the CR/CT specifications of SAS. At the time of release of this specification, the External Data Center Cable/Connector is designed in a manner that allows it to be plugged into a SAS domain. However, SAS systems compatible with the T10/1562-D standard, including those that support attachment and control of SATA devices, do not necessarily operate with SATA systems that include functions such as Port Selectors, Port Multipliers or Serial ATA Switches. This potential interoperability issue may be resolved in the future. The reader is cautioned to investigate these issues carefully before deploying these systems.

6.1.7.9 Potential External SATA Incompatibility Issues

WARNING: The functionality of External Desktop and External DataCenter cabled applications is not defined by any Serial ATA Specification. Consequently, two systems could be connected which may not interoperate even though all the components comply with the PHY specifications of this document. SATA II concepts such as Switches, Port Multipliers and Port Selectors are defined in various SATA II specifications but External Applications are not required to support these constructs. As a result, a Host with an External Data Center connector could be connected to a Disk Array containing a SATA Switch and the resulting system may not operate correctly.

6.1.7.10 Notebook Applications

The Serial ATA II Committee does not specifically include applications for Serial ATA devices within or connected to Notebook computers although the committee acknowledges this application as important. If any proprietary cables/connectors or electrical specifications are developed for this application, the system shall be designed so as to prevent connection with standard SATA components. If standard cables/connectors/electrical interfaces are used within the Notebook, within the Docking Bay or to External Storage Components, these shall comply with the appropriate Serial ATA specifications and interoperate properly with Serial ATA components.

Internal Applications:
It is anticipated that all internal interfaces may comply with the Gen1i and Gen2i specifications. Any Notebook designer modifying electrical specifications of Hosts and Devices within the Notebook is free to do so, however, all proprietary interfaces shall be designed so as to prevent connection with standard SATA components.

Docking Bay Applications:
All proprietary Docking Bay interfaces shall be designed so as to prevent connection with standard SATA components.

External Applications:
Applications for external Serial ATA interfaces on Notebook computers may use either the External Desktop Cable/Connector (Gen1m at 1.5 Gb/s, Gen2x at 3.0 Gb/s) or the System-to-System Data Center Cable/Connector (Gen1x at 1.5 Gb/s or Gen2x at 3.0 Gb/s). If a proprietary solution is developed it shall be designed so as to prevent connection with standard SATA components.

6.1.8 Low level electronics block diagram-[Informative]

6.1.8.1 Diagram-[Informative]

The following block diagrams are provided as a reference for the following sections of this document. Although informative in nature, the functions of the blocks described herein provide the basis upon which the normative specifications apply. The individual blocks provided are considered the “industry standard” way to approach this design and are provided as an example of one possible implementation.

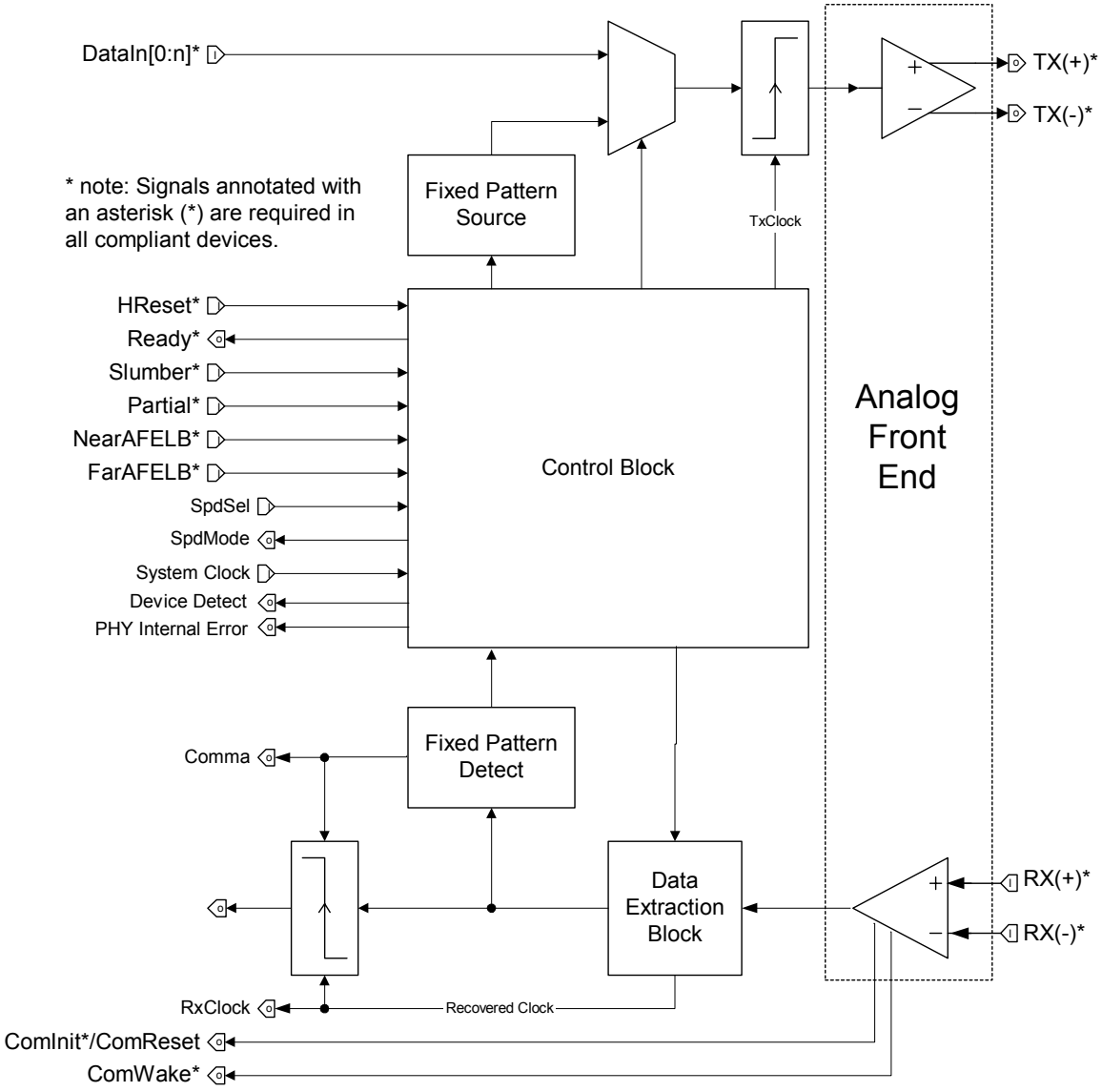


Figure 7: Physical plant overall block diagram-[Informative]

6.1.8.2 Physical plant overall block diagram description-[Informative]

Analog front end	This block is the basic interface to the transmission line. This block consists of the high speed differential drivers and receivers as well as the Out Of Band signaling circuitry.
Control block	This block is a collection of logic circuitry that controls the overall functionality of the Physical plant circuitry.
Fixed pattern source	This block provides the support circuitry that generates the patterns as needed to implement the ALIGN primitive activity.
Fixed pattern detect	This block provides the support circuitry to allow proper processing of the ALIGN primitives.
Data extraction block	This block provides the support circuitry to separate the clock and data from the high speed input stream.
TX clock	This signal is internal to the Physical plant and is a reference signal that regulates the frequency at which the serial stream is sent via the high speed signal path
TX + / TX -	These signals are the outbound high speed differential signals that are connected to the serial ATA cable.
RX + / RX -	These signals are the inbound high speed differential signals that are connected to the serial ATA cable.
DATAIN	Data sent from the Link layer to the Phy layer for serialization and transmission.
PHYRESET	This input signal causes the PHY to initialize to a known state and start generating the COMRESET Out Of Band signal across the interface.
PHYRDY	Signal indicating Phy has successfully established communications. The Phy is maintaining synchronization with the incoming signal to its receiver and is transmitting a valid signal on its transmitter.
SLUMBER	Causes the Phy layer to transition to the Slumber power management state.
PARTIAL	Causes the Phy layer to transition to the Partial power management state
NEARAFELB	Causes the Phy to loop back the serial data stream from its transmitter to its receiver
FARAFELB	Causes the Phy to loop back the serial data stream from its receiver to its transmitter
SPDSEL	Causes the control logic to automatically negotiate for a usable interface speed or sets a particular interface speed. The actual functionality of this input is vendor specific and varies from manufacturer to manufacturer.
SPDMODE	Output signal that reflects the current interface speed setting. The actual functionality of this signal is vendor specific and varies from manufacturer to manufacturer.

SYSTEMCLOCK This input is the clock source for much of the control circuit and is the basis from which the transmitting interface speed is established.

COMMA This signal indicates that a K28.5 character was detected in the inbound high speed data stream.

DATAOUT Data received and de-serialized by the Phy and passed to the Link layer

RX CLOCK / Recovered clock - This signal is derived from the high speed input data signal and determines when parallel data has been properly formed at the DATAOUT pins and is available for transfer to outside circuitry.

COMRESET / COMINIT
Host: Signal from the Out Of Band detector that indicates the COMINIT Out Of Band signal is being detected.
Device: Signal from the Out Of Band detector that indicates the COMRESET Out Of Band signal is being detected.

COMWAKE Signal from the Out Of Band detector that indicates the COMWAKE Out Of Band signal is being detected.

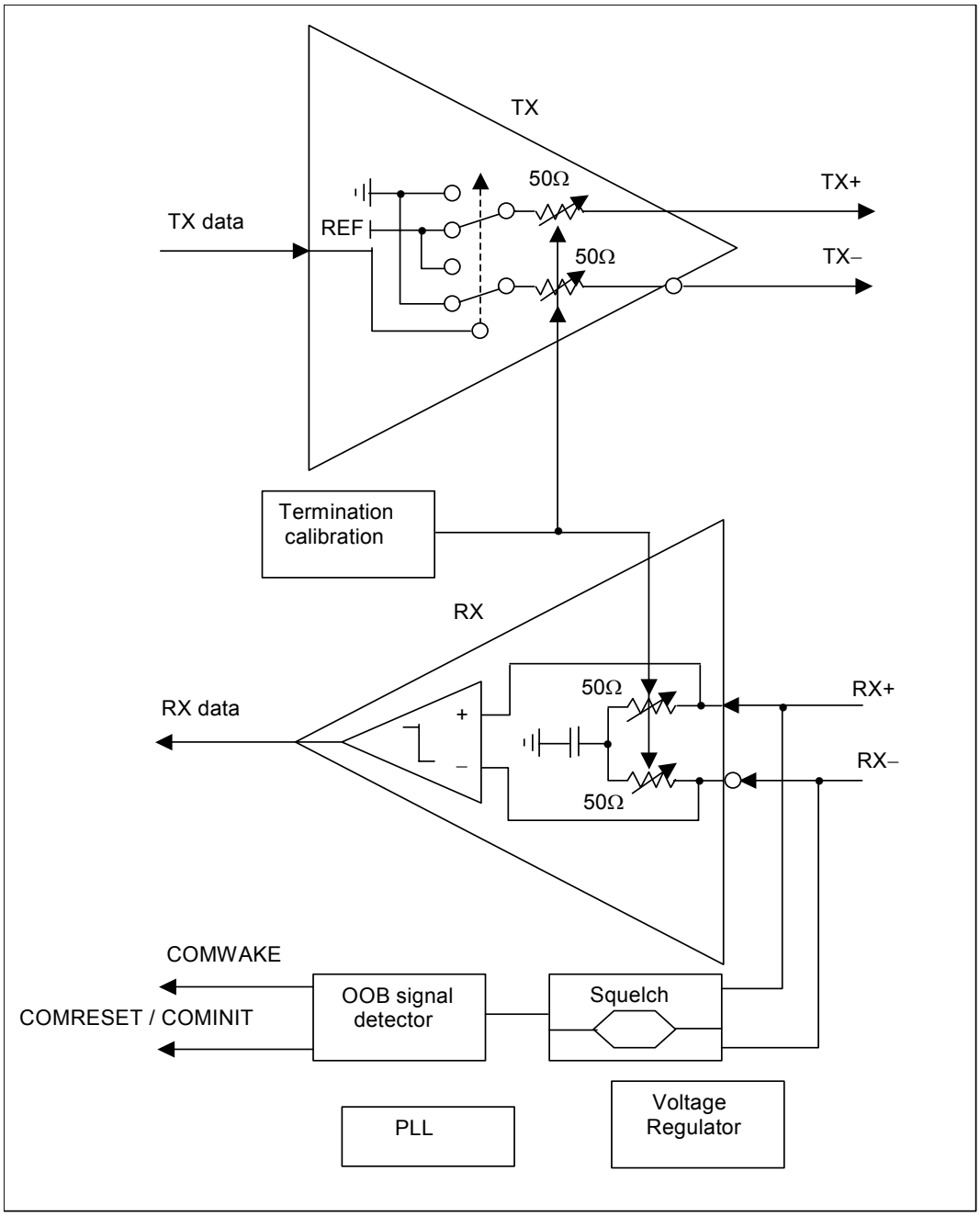


Figure 8: Analog front end (AFE) block diagram-[Informative]

[External AC caps not shown]

6.1.8.3 Analog front end (AFE) block diagram description-[Informative]

TX	This block contains the basic high speed driver electronics
RX	This block contains the basic high speed receiver electronics
Termination calibration	This block is used to establish the impedance of the RX block in order to properly terminate the high speed serial cable.
Squelch	This block establishes a limit so that detection of a common mode signal can be properly accomplished.
OOB signal detector	This block decodes Out Of Band signal from the high speed input signal path.
PLL	This block is used to synchronize an internal clocking reference so that the input high speed data stream may be properly decoded.
Voltage Regulator	This block stabilizes the internal voltages used in the other blocks so that reliable operation may be achieved. This block may or may not be required for proper operation of the balance of the circuitry. The need for this block is implementation specific.
TX+ / TX-	This is the same signal as described in the previous section: Physical plant overall block diagram description
RX+ / RX-	This is the same signal as described in the previous section: Physical plant overall block diagram description
TxData	Serially encoded 10b data attached to the high speed serial differential line driver.
RxData	Serially encoded 10b data attached to the high speed serial differential line receiver.
COMWAKE	This is the same signal as described in the previous section: Physical plant overall block diagram description
COMRESET / COMINIT	This is the same signal as described in the previous section: Physical plant overall block diagram description

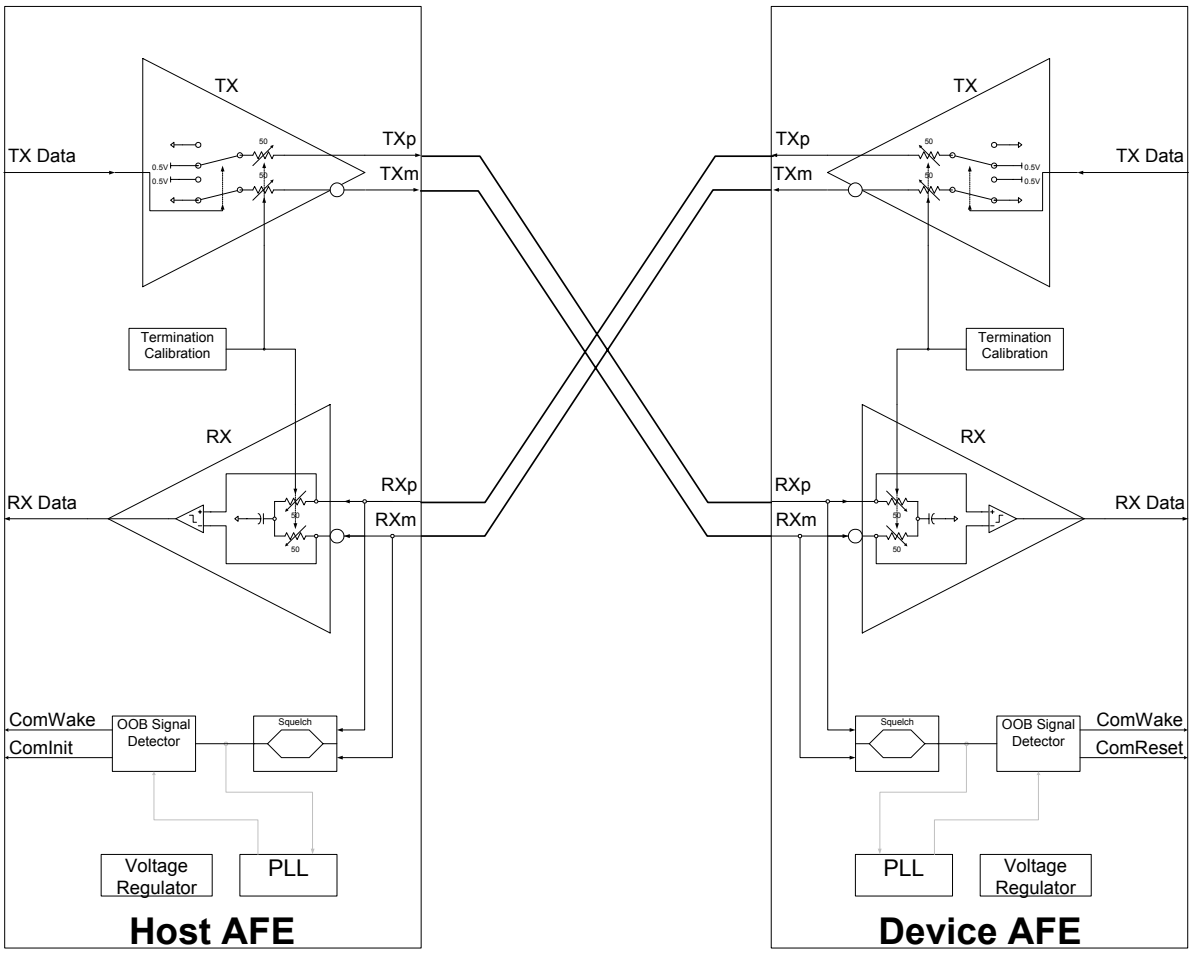


Figure 9: Analog front end (AFE) cabling-[Informative]

[External AC Coupling Capacitors not shown]

6.1.9 Compliance Testing

This document provides electrical specifications that when met by Hosts, Devices, and Interconnects, satisfy the link performance specifications when combined into a system. This section of the document provides an overview of how to determine whether a Host, Device, or Interconnect is compliant to the specifications of this document.

Each electrical specification requires a specific measurement, test setup and data patterns. This section ties all of these requirements together to aid the reader in understanding what is needed for compliance testing.

Table 2, Table 3, Table 4, Table 5, Table 6, and Table 7 detail the electrical requirements for SATA compliance. Each requirement is defined in Section 6.2.2. Jitter is described in Section 6.3. Measurement methods for each specification are detailed in Section 6.4. Section 6.5 discusses Interface States relating to Out Of Band (OOB) and power management. Section 6.6 describes the Interconnect requirements.

A Serial ATA system is divided into components. There are three types of components:

- Hosts
- Devices
- Interconnect

The SATA link is a full duplex point to point link as continuous data activity exists on each direction. For purposes of compliance testing of Hosts and Devices, the full duplex link is broken into two simplex links, one for the Host transmitting to the Device and the other for the Device transmitting to the Host. Each link is tested for compliance separately. Each transmitter to receiver Link contains the following elements:

Transmitter (IC/PCB/SATA Connector) – to –
Interconnect (Connector/Cable or PCB/Connector) – to –
Receiver (SATA Connector / PCB / IC)

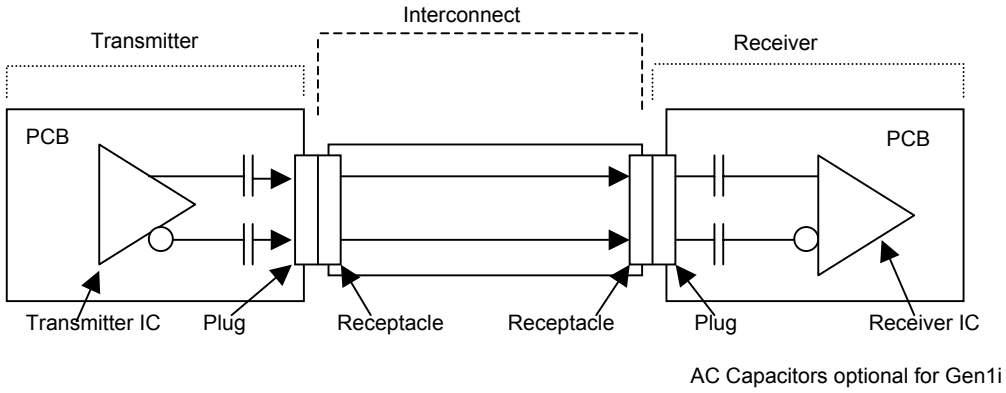


Figure 10: The Simplex Link

In testing the compliance of SATA components that make up a system there are five Compliance Areas to be measured:

1. “Transmitted Signal”– Examine the transmitted signal quality at the compliance point for the Host/Device into a Laboratory Load. Electrical specifications include amplitude, rise/fall time, frequency, jitter, etc. The Electrical specifications apply to the signal output from the Transmitter-Under-Test at the mated connector when driving a Laboratory Load. No attempt has been made to specify the signal when attached to a cable, backplane or directly into another Device. Actual signals “In-System” will vary.
2. “Transmitter” – Examine all specified characteristics of the Transmitter from the compliance point. This includes specifications such as differential and common-mode impedance. The “Transmitter” includes the IC which incorporates the transmitter, the PCB, the SATA connector as well as any additional components between the IC and the SATA connector.
3. “Receiver” – Examine all specified characteristics of the Receiver from the compliance point. This includes specifications such as differential and common-mode impedance. The “Receiver” includes the SATA connector, the PCB and the IC which incorporates the receiver as well as any additional components between the IC and the SATA connector.
4. “Receiver Tolerance” – When the Receiver is presented with a worst-case “Lab-Sourced Signal”, and operating with its active transmitter, shall meet the specified Frame Error Rates. This requires carefully controlled signal sources in order to generate a worst-case signal.
5. "Interconnect" -- Examine all specified characteristics of the interconnect using test equipment. The interconnect includes SATA connector pairs at each end. The testing requirements and procedures are described in section 6.6.

In order to determine compliance to the specifications of this document, measurements shall be performed separately with Host, Device, or Interconnect being tested when connected to test equipment. Compliance tests are not done with a Host, Device, or Interconnect connected together. Unless otherwise specified, all compliance measurements shall be taken through the mated connector pair.

NOTE: The electrical specifications in the Receiver Tolerance Table DO NOT describe the characteristics of the received signal; these describe the Lab-Sourced Signal calibrated into a Laboratory Load and subsequently applied to the Receiver. The Receiver Tolerance Table DOES NOT describe the characteristics of a signal from a Transmitter through an Interconnect into a Laboratory Load. Received signals in a system are potentially worse due to the non-ideal impedance match of Transmitter and Receiver.

6.1.10 Link Performance

The performance of a SATA system with Host and Device linked together with an Interconnect is measured by the frame error rate, using a set of reference frames, defined by a specific set of ordered test patterns within the frame. An operating Host-Device duplex link that meets the Frame Error Rate (FER) specifications of Table 2 for both of its simplex links is deemed to fulfill Serial ATA performance levels. A Host or Device is commanded to generate the various test patterns through the use of the BIST FIS Serial ATA command or other vendor unique commands to the device under test.

6.1.11 Physical Layer Definitions

BER Bit Error Rate

BERT Bit error rate tester. A device capable of error measurement at Gen1 or Gen2 data rates.

Bitrate Reciprocal of the unit interval, bitrate = 1 / UI.

Burst A short pulse of data starting from and ending with the idle condition on the interface. These are used for OOB signaling.

Data Signal Source An instrument which provides a Serial ATA data signal.

DCB The DC block is defined as a device that will pass frequencies from 10 MHz to at least 12 GHz with minimal effect on the amplitude or phase of the signal.

Differential Signal The differential signal is the voltage on the positive conductor minus the voltage on the negative conductor (i.e. TX+ – TX-).

DJ Deterministic Jitter (peak to peak). All jitter sources that have bounded probability distribution functions (i.e. values outside the bounds have probability zero). Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent (ISI), sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value.

Fbaud The nominal rate of data through the channel.

FER Frame Error Rate

Gen1i The inside-the-box electrical specifications for Serial ATA 1.0a at 1.5Gb/s with cable lengths up to 1m.

Gen2i The inside-the-box electrical specifications newly defined in this document at 3.0Gb/s with cable lengths up to 1m.

Gen1m The electrical specifications used in the “Short” Backplane application and the External Desktop application which were defined in “Serial ATA II: Extensions to Serial ATA 1.0” revision 1.0 dated October 16, 2002. Only the Transmitter and Receiver Differential Swing specifications were modified. All other electrical specifications are identical to Gen1i.

Gen2m The electrical specifications used in the “Short” Backplane appliction and the External Desktop application which are defined in this document. Only the Transmitter and Receiver Differential Swing specifications were modified. All other electrical specifications are identical to Gen2i.

Gen1x The outside-the-box cabled applications or "Long" backplane applications defined at 1.5Gb/s.

Gen2x The outside-the-box cabled applications or "Long" backplane applications defined at 3.0Gb/s.

HBWS High Bandwidth Scope. An oscilloscope with an analog bandwidth of 10 GHz or greater in the measurement path.

HFTP High Frequency Test Pattern. This pattern provides the maximum frequency allowed within the Serial ATA encoding rules. Pattern: 1010101010 1010101010b = encoded D10.2. The pattern is repetitive.

ISI Inter-symbol interference. Data-dependent deterministic jitter caused by the time differences required for the signal to arrive at the receiver threshold when starting from different places in bit sequences (symbols). For example media attenuates the peak amplitude of the bit sequence [0,1,0,1...], more than it attenuates the peak amplitude of the bit sequence [0,0,0,0,1,1,1,1...], thus the time required to reach the receiver threshold with the [0,1,0,1...] sequence is less than required from the [0,0,0,0,1,1,1,1...]sequence. The run length of 4 produces a higher amplitude which takes more time to overcome when changing bit values and therefore produces a time difference compared to the run length of 1 bit sequence. When different run lengths are mixed in the same transmission the different bit sequences (symbols) therefore interfere with each other. ISI is expected whenever any bit sequence has frequency components that are propagated at different rates by the transmission media. This translates into a high level of high-frequency, data-dependent, jitter.

JMD Jitter Measuring Device. A device used to measure jitter. Examples are a bit error rate tester (BERT), a timing interval analyzer (TIA), a single shot capture oscilloscope and processing software, or a HBWS.

LBP Lone bit pattern. This pattern is defined in section 6.2.4.3.5. The pattern is repetitive.

LFTP Low Frequency Test Pattern. This pattern provides a low frequency, which is allowed within the Serial ATA encoding rules. Pattern: 0111100011 1000011100b = encoded D30.3. The pattern is repetitive.

LL Laboratory Load. An electrical test system connected to the unit under test. The serial transmitter signals from the UUT are connected through a “mated SATA connector pair” module consisting of connectors and cables to a HBWS terminated into two 50 ohms (plus and minus 5 ohms) loads. The Cables shall be 50 ohms (plus and minus 5 ohms) impedance. The inputs of the Laboratory Load (from the back of the mated SATA connector to the 50 ohm load within the HBWS) shall have an individual return loss greater than 20 dB over a bandwidth of 100 MHz to 5.0 GHz, and greater than 10 dB from 5GHz to 8GHz. The skew between the channels under test shall have 10 Picoseconds or less after compensation. The LL consists of this total assembly. The LL does NOT include the “other ½ of the mated connector” which is considered part of the UUT but is physically located on the LL. The LL is shown in Figure 11.

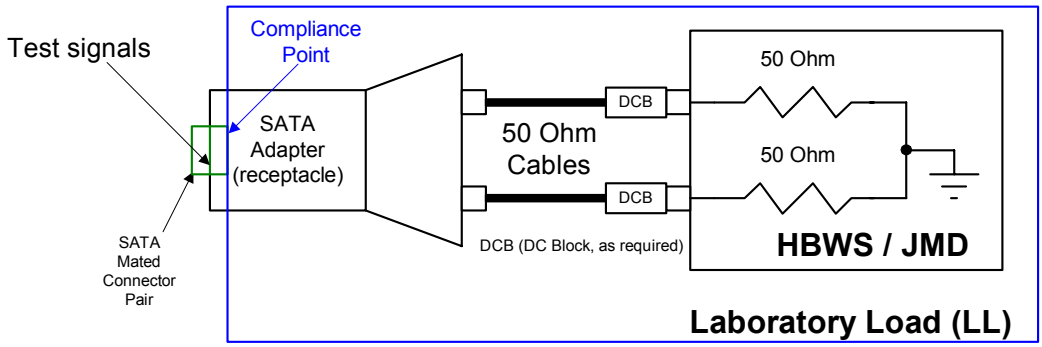


Figure 11: LL Laboratory Load

The electrical characteristics of the LL shall be greater than the required performance of the parameter being measured such that its effects of the on the parameter under test can be successfully compensated for, or de-embedded, in the measured data.

LSS Laboratory Sourced Signal or Lab-Sourced Signal. An instrument and electrical test system connected to the unit under test. The LSS provides a signal to the UUT at the defined impedance level of 100 ohms differential and 25 ohms common mode. The LSS may also

provide a SATA signal with impairments such as jitter and common mode noise. The LSS may consist of several instruments in combination with fixturing to create a signal with impairments.

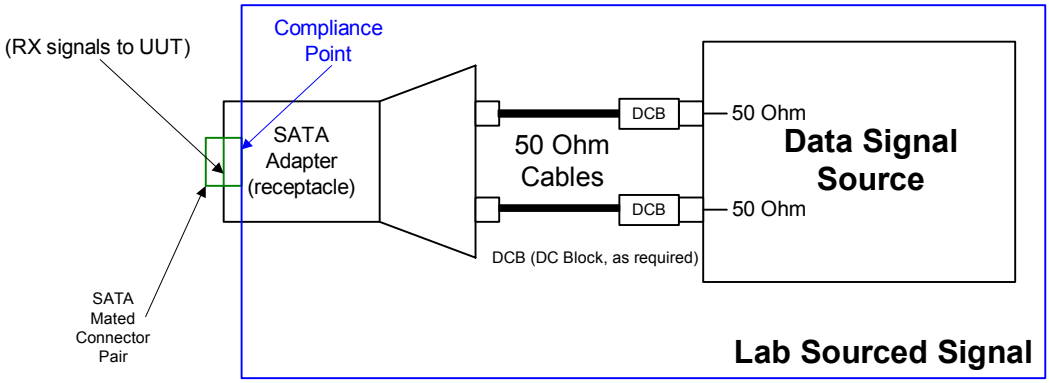


Figure 12: LSS Lab-Sourced Signal

Max Maximum value is the highest value of the waveform.

Min Minimum value is the lowest value of the waveform.

MFTP Mid Frequency Test Pattern. This pattern provides a middle frequency which is allowed within the Serial ATA encoding rules. Pattern: 1100110011 0011001100b = encodedD24.3. The pattern is repetitive.

OS-Aware Hot Removal This is defined as the removal of a SATA Device from a powered backplane, that has been first placed in a quiescent state.

OS-Aware Hot Plug This is defined as the insertion of a SATA Device into a backplane that has power shutdown. The backplane is later powered, and both the device and the host power up, and the Host-initiated OOB sequence will determine the time at SATA operations begin.

Peak to Peak Peak to Peak = Max Value – Min Value

RJ Random Jitter (peak to peak). Defined to be Gaussian and equal to 14 times the 1σ standard deviation value given the 10^{-12} BER requirement.

SSC Spread Spectrum Clocking. The technique of modulating the operating frequency of a signal slightly to spread its radiated emissions over a range of frequencies. This reduction in the maximum emission for a given frequency helps meet radiated emission requirements.

Surprise Hot Plug This is defined as the insertion of a SATA Device into a backplane that has power present. The device powers up and initiates an OOB sequence.

Surprise Hot Removal This is defined as the removal of a SATA Device from a powered backplane, without first being placed in a quiescent state.

TDR Time Domain Reflectometer. An instrument used to test the impedance of the unit under test.

TJ Total Jitter (peak to peak). Defined to be DJ + RJ.

UI Unit Interval. Equal to the time required to transmit one bit (666.667 ps for Gen1).

TIA Timing interval analyzer with DCD&ISI noise floor performance of better than 5% of a UI for K28.5 with less than 67ps rise and fall times.

UUT Unit under test. This is to include the product under test and the other ½ of the “mated “connector (which is physically on the Laboratory Load but considered part of the UUT.

VNA Vector Network Analyzer. An instrument used to test the impedance of the unit under test.

Zero Crossing To locate the Zero Crossing of a Data Eye, turn on the horizontal histogram function to horizontally enclose all waveforms associated with the “edge” and vertically limit to +/-5% of the waveform voltage. The “Zero Crossing” is the location of the mean of the waveforms.

6.2 Electrical specifications

The goal of this specification is to provide a description of characteristics to ensure interoperability of SATA components; devices, hosts, and interconnects. Any combination of compliant components should provide the stated link performance. Secondly a means of validation to the requirements is described in Section 6.4. Validation consists of performing tests on individual SATA components.

Serial ATA devices and hosts shall comply with the electrical specifications shown in Table 2, Table 3, Table 4, Table 5, Table 6, and Table 7. The transmitter consists of the driver, printed circuit board, and mated connector pair. The receiver consists of the receiver IC, printed circuit board, and mated connector pair.

Unless otherwise stated, all specifications include the mated connector pair.

6.2.1 Physical Layer Requirements Tables

Table 2: General Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Channel Speed	Gbs	Nom	1.5			3.0			6.2.2.1.1	-
Fbaud	GHz	Nom	1.5			3.0			-	-
FER, Frame Error Rate		Max	8.2e-8 at 95% confidence level			8.2e-8 at 95% confidence level			6.2.2.1.2	6.4.1
T_{UI}, Unit Interval	ps	Min	666.4333			333.2167			6.2.2.1.3	6.4.11
		Nom	666.6667			333.3333				
		Max	670.2333			335.1167				
f_{tol}, TX Frequency Long Term Stability	ppm	Min	-350			-350			6.2.2.1.4	6.4.6
		Max	+350			+350				
f_{ssc}, Spread-Spectrum Modulation Frequency	kHz	Min	30			30			6.2.2.1.5 6.3.3	6.4.11
		Max	33			33				
SSC_{tol}, Spread-Spectrum Modulation Deviation	ppm	Min	-5000			-5000			6.2.2.1.6 6.3.3	6.4.11
		Max	+0			+0				
$V_{cm,dc}$, DC Coupled Common Mode Voltage	mV	Min	200		-	-			6.2.2.1.7	6.4.4
		Nom	250		-	-				
		Max	450		-					
$V_{cm,ac\ coupled}$, AC Coupled Common Mode Voltage	mV	Min	0		-	-			6.2.2.1.8	6.4.25
		Max	2000		-	-				
Z_{diff}, Nominal Differential Impedance	ohm	Nom	100		-	-			6.2.2.1.9	6.4.22

$C_{ac\ coupling}$ AC Coupling Capacitance	nF	Max	12		12	6.2.2.1.10	6.4.14
$t_{settle,cm}$, Common Mode Transient Settle Time	ns	Max	10	-	-	6.2.2.3.6	-
V_{trans}, Sequencing Transient Voltage	V	Min	-2.0		-2.0	6.2.2.1.11	6.4.13
		Max	2.0		2.0		

Table 3: Transmitter Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Z_{diffTX}, TX Pair Differential Impedance	Ohm	Min	85		85	-		85	6.2.2.2.1	6.4.22
		Max	115		115	-		115		
$Z_{s\text{-}eTX}$, TX Single-Ended Impedance	Ohm	Min	40		-	-			6.2.2.2.2	6.4.23
$RL_{DD11,TX}$, TX Differential Mode Return Loss (all values Min)	dB	150MHz-300MHz	-			14	14	-	6.2.2.2.3	6.4.10
		300MHz-600MHz	-			8	8	-		
		600MHz-1.2GHz	-			6	6	-		
		1.2GHz-2.4GHz	-			6	6	-		
		2.4GHz-3.0GHz	-			3	3	-		
		3.0GHz-5.0GHz	-			1	-	-		
$RL_{CC11,TX}$, TX Common Mode Return Loss (all values Min)	dB	150MHz-300MHz	-			8	5	-	6.2.2.2.4	6.4.10
		300MHz-600MHz	-			5	5	-		
		600MHz-1.2GHz	-			2	2	-		
		1.2GHz-2.4GHz	-			2	2	-		
		2.4GHz-3.0GHz	-			2	1	-		
		3.0GHz-5.0GHz	-			1	-	-		

$RL_{DC11,TX}$, TX Impedance Balance (all values Min)	dB	150MHz-300MHz	-	30	30	-	6.2.2.2.5	6.4.10
		300MHz-600MHz	-	20	20	-		
		600MHz-1.2GHz	-	10	10	-		
		1.2GHz-2.4GHz	-	10	10	-		
		2.4GHz-5.0GHz	-	4	4	-		
		2.4GHz-5.0GHz	-	4	-	-		

Table 4: Transmitted Signal Requirements

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{diffTX}, TX Differential Output Voltage	mVppd	Min	400	500	800	400	500	800	6.2.2.3.1	6.4.4
		Nom	500		-	-				
		Max	600		1600	700		1600		
UI_{VminRX}, TX Minimum Voltage Measurement Interval	UI		-		0.5	0.45-0.55		0.5	6.2.2.3.2	6.4.4
$t_{20\text{-}80TX}$, TX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		67 (.10)	67 (.20)			6.2.2.3.3	6.4.3
		Max 20-80%	273 (.41)		273 (.41)	136 (.41)				
t_{skewTX}, TX Differential Skew	ps	Max	20			20		15	6.2.2.3.4	6.4.12
$V_{cm,acTX}$, TX AC Common Mode Voltage	mVp-p	Max	-			50		-	6.2.2.3.5	6.4.17
$D_{VdiffOOB}$, OOB Differential Delta	mV	Max	-		25	25			6.2.2.3.7	6.4.19
D_{VcmOOB}, OOB Common Mode Delta	mV	Max	-		50	50			6.2.2.3.8	6.4.18
R/F_{bal}, TX Rise/Fall Imbalance	%	Max	-			20		-	6.2.2.3.9	6.4.16
Amp_{bal}, TX Amplitude Imbalance	%	Max	-		10	10			6.2.2.3.10	6.4.15

TJ at Connector, Data-Data, 5UI	UI	Max	0.355	-	-		6.2.2.3.11 6.3	-
DJ at Connector, Data-Data, 5UI	UI	Max	0.175	-	-			
TJ at Connector, Data-Data, 250UI	UI	Max	0.47	-	-			
DJ at Connector, Data-Data, 250UI	UI	Max	0.22	-	-			
TJ at Connector, Clk-Data, f_{BAUD}/10	UI	Max	-		0.30	-	6.2.2.3.12 6.3	6.4.7 6.4.8
DJ at Connector, Clk-Data, f_{BAUD}/10	UI	Max	-		0.17	-		
TJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-		0.37	-		
DJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-		0.19	-		
TJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-	0.55	-	0.55		
DJ after CIC, Clk-Data, f_{BAUD}/1667	UI	Max	-	0.35	-	0.35		

Table 5: Receiver Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
Z_{diffRX}, RX Pair Differential Impedance	Ohm	Min	85			-		85	6.2.2.4.1	6.4.22
		Max	115			-		115		
Z_{s-eRX}, RX Single-Ended Impedance	Ohm	Min	40		-	-			6.2.2.4.2	6.4.23
$RL_{DD11,RX}$, RX Differential Mode Return Loss (all values are Min)	dB	150MHz-300MHz	-			18	18	-	6.2.2.4.3	6.4.10
		300MHz-600MHz	-			14	14	-		
		600MHz-1.2GHz	-			10	10	-		
		1.2GHz-2.4GHz	-			8	8	-		
		2.4GHz-3.0GHz	-			3	3	-		
		3.0GHz-5.0GHz	-			1	-	-		
$RL_{CC11,RX}$, RX Common Mode Return Loss (all values are Min)	dB	150MHz-300MHz	-			5	5	-	6.2.2.4.4	6.4.10
		300MHz-600MHz	-			5	5	-		
		600MHz-1.2GHz	-			2	2	-		
		1.2GHz-2.4GHz	-			2	2	-		
		2.4GHz-3.0GHz	-			2	1	-		
		3.0GHz-5.0GHz	-			1	-	-		
$RL_{DC11,RX}$, RX Impedance Balance (all values are Min)	dB	150MHz-300MHz	-			30	30	-	6.2.2.4.5	6.4.10
		300MHz-600MHz	-			30	30	-		
		600MHz-1.2GHz	-			20	20	-		
		1.2GHz-2.4GHz	-			10	10	-		
		2.4GHz-3.0GHz	-			4	4	-		
		3.0GHz-5.0GHz	-			4	-	-		

Table 6: Lab-Sourced Signal (for Receiver Tolerance Testing)

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{diffRX}, RX Differential Input Voltage	mVppd	Min	325	240	275	275	240	275	6.2.2.5.1	6.4.5
		Nom	400		-					
		Max	600		1600	750	750	1600		
$t_{20\text{-}80RX}$, RX Rise/Fall Time	ps (UI)	Min 20-80%	100 (.15)		67 (.10)	67 (.20)			6.2.2.5.2	6.4.3
		Max 20-80%	273 (.41)			136 (.41)				
UI_{VminRX}, RX Minimum Voltage Measurement Interval	UI		-		0.5	0.5			6.2.2.5.3	6.4.5
t_{skewRX}, RX Differential Skew	ps	Max	-		80	50		75	6.2.2.5.4	6.4.12
$V_{cm,acRX}$, RX AC Common Mode Voltage	mVp-p	Max	100		150	100		150	6.2.2.5.5	6.4.9
$f_{cm,acRX}$, AC Common Mode Frequency	MHz.	Min	2			2			6.2.2.5.6	6.4.9
		Max	200			200				
TJ at Connector, Data-Data, 5UI	UI	Max	0.43		-				6.2.2.5.7 6.3	-
DJ at Connector, Data-Data, 5UI	UI	Max	0.25		-					
TJ at Connector, Data-Data, 250UI	UI	Max	0.6		-					
DJ at Connector, Data-Data, 250UI	UI	Max	0.35		-	-				

TJ at Connector, Clk-Data, f_{BAUD}/10	UI	Max	-		0.46	-	6.2.2.5.8 6.3	6.4.7 6.4.9
DJ at Connector, Clk-Data, f_{BAUD}/10	UI	Max	-		0.35	-		
TJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-		0.60	-		
DJ at Connector, Clk-Data, f_{BAUD}/500	UI	Max	-		0.42	-		
TJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-	0.65	-	0.65		
DJ at Connector, Clk-Data, f_{BAUD}/1667	UI	Max	-	0.35	-	0.35		

Table 7: OOB Specifications

Parameter	Units	Limit	SATA Usage Model						Detail Cross-Ref Section	Meas. Cross-Ref Section
			Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x		
V_{thresh}, OOB Signal Detection Threshold	mVppd	Min	50		120	75		120	6.2.2.6.1	6.4.20
		Nom	100		-	125		-		
		Max	200		240	200		240		
UI_{OOB}, UI During OOB Signaling	ps	Min	646.67			646.67			6.2.2.6.2	-
		Nom	666.67			666.67				
		Max	686.67			686.67				
COMINIT/ COMRESET and COMWAKE Transmit Burst Length	UI_{OOB}		160			160			6.2.2.6.3	6.4.21
COMINT/ COMRESET Transmit Gap Length	UI_{OOB}		480			480			6.2.2.6.4	6.4.21
COMWAKE Transmit Gap Length	UI_{OOB}		160			160			6.2.2.6.5	6.4.21
COMWAKE Gap Detection Windows	ns	May detect	55 ≤ T < 175			55 ≤ T < 175			6.2.2.6.6	6.4.21
		Shall detect	101.3 ≤ T ≤ 112			101.3 ≤ T ≤ 112				
		Shall not detect	T < 55 or T ≥175			T < 55 or T ≥175				
COMINIT/ COMRESET Gap Detection Windows	ns	May detect	175 ≤ T < 525			175 ≤ T < 525			6.2.2.6.7	6.4.21
		Shall detect	304 ≤ T ≤ 336			304 ≤ T ≤ 336				
		Shall not detect	T < 175 or T ≥ 525			T < 175 or T ≥ 525				

6.2.2 Physical Layer Requirements Details

6.2.2.1 General Specifications Details

This section contains the details on Table 2 entries.

6.2.2.1.1 Channel Speed

A reference value showing the nominal rate of data through the channel.

6.2.2.1.2 Frame Error Rate

Frame error rate is the measure of link performance using all the intermediate circuit blocks in the chain from low-level Phy Layer, Link Layer, through Transport Layer. Frame error rate is a system level test, not a compliance test. Error detection is at the frame level using the CRC (Cyclic Redundancy Check) error detection mechanism, and respective reporting to the higher layer levels.

6.2.2.1.3 Unit Interval

This is the operating data period (nominal value architecture specific). This value includes the long term frequency accuracy and the Spread Spectrum Clock FM frequency deviation (rounded to 4 places).

This is the time interval value of each cycle of the Reference Clock.

6.2.2.1.4 TX Frequency Long Term Stability

This specifies the allowed frequency variation from nominal; this does not include frequency variation due to jitter, Spread Spectrum Clocking, or phase noise of the clock source.

6.2.2.1.5 Spread-Spectrum Modulation Frequency

The modulation frequency of the Spread-Spectrum frequency modulation. See further details of Spread-Spectrum in Section 6.3.3.

6.2.2.1.6 Spread-Spectrum Modulation Deviation

This is the allowed frequency variation from nominal due to the SSC AC modulation expressed in terms of the unit interval deviation from the unit interval value of the long term frequency value. See further details of Spread-Spectrum in Section 6.3.3.

6.2.2.1.7 DC Coupled Common Mode Voltage (Gen1i)

The Common mode DC level is defined as [(TX+) + (TX-)]/2 and [(RX+) + (RX-)]/2 measured at the mated connector.

This requirement only applies to Gen1i DC-coupled designs (no blocking capacitors) that hold the common-mode DC level at the connector. The four possible common mode biasing configurations shown in Figure 13 below demonstrate that only DC-coupled designs need sustain the specified common-mode level to ensure interoperability. AC coupled designs may allow the DC level at the connector to float. The SATA interfaces defined as Gen1x, Gen2i, Gen2x shall be AC-coupled and this requirement does not apply to these.

A DC-coupled receiver shall weakly hold the common-mode level of its inputs to the $V_{cm,dc}$ value specified in Table 2. A DC-coupled transmitter shall transmit with the $V_{cm,dc}$ value specified in Table 2 while driving into a 100 ohm differential impedance.

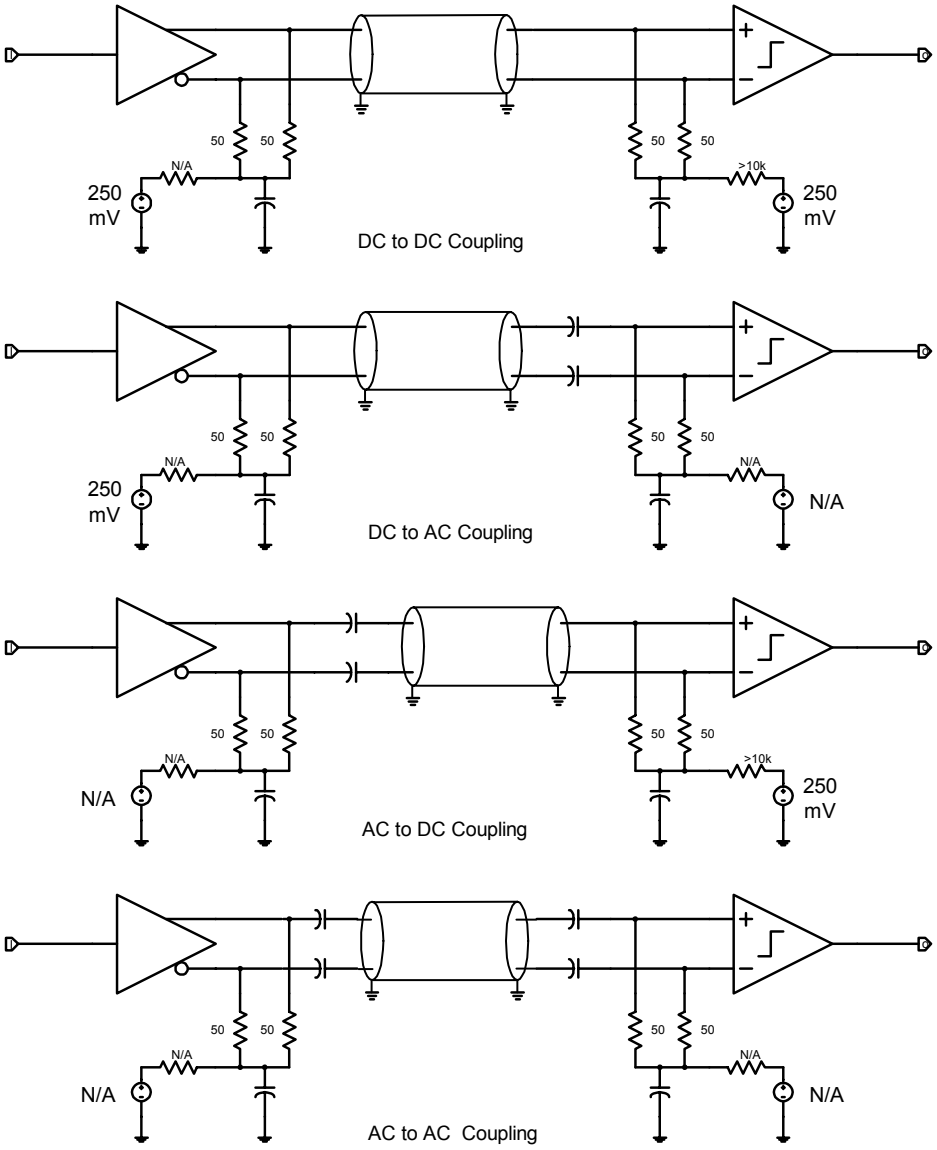


Figure 13: Common mode biasing examples for Gen1i [Informative]

6.2.2.1.8 AC Coupled Common Mode Voltage

The SATA interface defined as Gen1i may be AC or DC coupled as shown in Figure 13. The SATA interfaces defined as Gen1x, Gen2i, Gen2x shall be AC-coupled. Figure 14 shows an example of a fully AC-coupled system.

Compliance points for SATA are defined at the connector. The AC coupled common mode voltage in Table 2 defines the open circuit DC voltage level of each single-ended signal at the IC side of the coupling capacitor in an AC coupled PHY and it shall be met during all possible power and electrical conditions of the PHY including power off and power ramping. Since the Gen1x, Gen2i, Gen2x specification defines only the signal characteristics as observable at the connector, this value is not applicable to those specifications. The common mode transient requirements defined in Table 2 were determined sufficient to limit stresses on the attached components under transient conditions which was the sole intent of the AC coupled common mode voltage requirement. Due to this, the following is true even for Gen1i where $V_{cm,ac\ coupled}$ applies: AC coupled common mode voltage levels outside the specified range may be used provided that the transient voltage requirements of Table 2 are met.

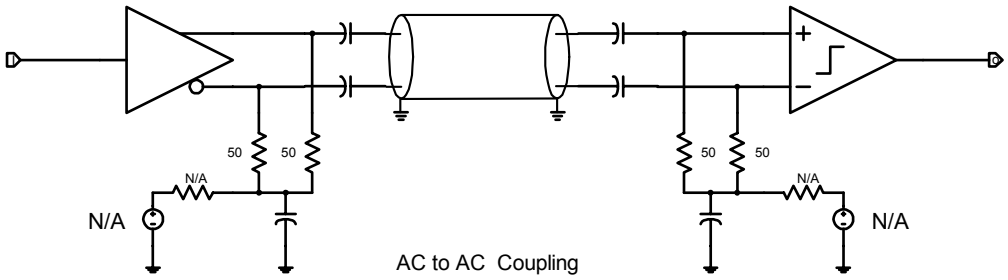


Figure 14: Common mode biasing for Gen1x, Gen2i, and Gen2x

6.2.2.1.9 Nominal Differential Impedance (Gen1i)

The Nominal impedance of all components in a SATA system.

6.2.2.1.10 AC Coupling Capacitance (Gen2i , Gen1x, Gen2x, optional for Gen1i)

The value of the coupling capacitor used in AC coupled implementations. AC Coupling is optional for Gen1i and mandatory of Gen1x, Gen2i, and Gen2x.

6.2.2.1.10.1 Coupling Capacitor Characteristics —[Informative]

The physical size of the capacitor should be as small as practical to reduce the capacitance to ground. Body sizes larger than 0603 (or values less than 300pF) should be avoided since they are likely to result in a failure of the return loss requirements in 6.2.2.2.3, and 6.2.2.4.3.

The physical size of the capacitor should be as small as practical to reduce the capacitance to ground. Body sizes larger than 0603 should be avoided as they are likely to result in a failure of the return loss requirements in Table 3 and Table 4.

6.2.2.1.11 Sequencing Transient Voltage

This parameter addresses the transient voltages on the serial data bus during power sequencing and power mode changes. Since either the receiver or the transmitter may be affected by power sequencing transients, the term "aggressor" is used to indicate the sequencing interface circuit and the term "victim" is used for the interface circuit receiving the transient.

In order to limit the voltage and energy seen by the victim receiver or transmitter circuitry during power sequencing, several parameters of the aggressor and victim are involved. Although parameters of the victim, such as common mode voltage and single ended impedance, affect the observed transient, this measurement addresses limiting the aggressor contribution.

The aggressor common mode voltage, single ended impedance, and AC coupling capacitor value determine the level of the sequencing transient. This measurement addressed the common mode voltage of the aggressor. The rate of change of the power on or power off ramp also affects this level. The limits provided allow for power up or power down ramps at rates faster than the time constants of the signal lines, although practical systems may not achieve this rate. This measurement shall include the test conditions of power on and power off ramping at the fastest possible rate expected in systems using the PHY, as well as any power mode transitions.

6.2.2.2 Transmitter Specification Details

This section contains the details on Table 3 entries.

6.2.2.2.1 TX Pair Differential Impedance (Gen1i)

As seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%). Measured with TDR in differential mode.

6.2.2.2.2 TX Single-Ended Impedance (Gen1i)

As seen by TDR with 100 ps (max) edge looking into connector (20%-80%). The TDR is set to produce simultaneous positive pulses on both signals of the TX pair. Single-ended impedance is the resulting (even mode) impedance of each signal. Both signals shall meet the single ended impedance requirement.

This requirement shall be met during all possible power and electrical conditions of the PHY including power off and power ramping.

6.2.2.2.3 TX Differential Mode Return Loss (Gen2i)

The differential mode return loss is defined as the ratio (expressed in dB) of differential mode incident power to differential mode reflected power both at a 100 ohm impedance level. In the system environment the purpose of controlling the return loss of devices and hosts is to limit signal reflections that cause data dependent jitter. These signal reflections in question are over and above those that exist in compliance testing when connected to a matched source or load.

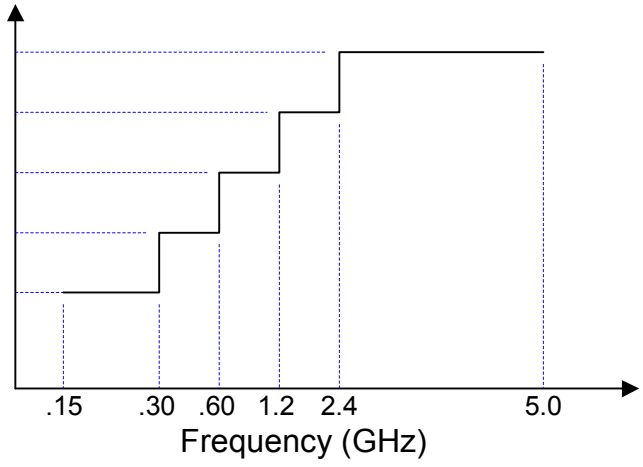


Figure 15: Differential Return Loss Limits

6.2.2.2.4 TX Common Mode Return Loss (Gen2i)

The common mode return loss is defined as the ratio (expressed in dB) of common mode incident power to common mode reflected power both at a 25 ohm impedance level. The intended signal propagation mode in SATA is the differential mode. However, imperfections in the system create some coupling between the common and differential modes. This has three consequences: radiated emissions, noise susceptibility, and signal degradation. Common mode reflections exacerbate these impairments. The common mode return loss is a bound on the magnitude of common mode reflections in the system.

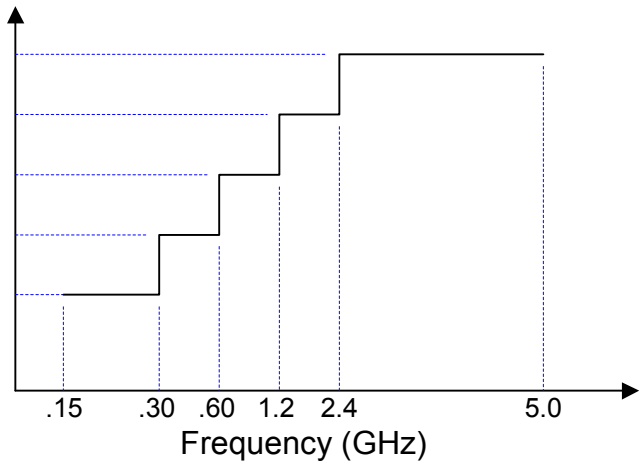


Figure 16: Common Mode Return Loss Limits

6.2.2.2.5 TX Impedance Balance (Gen2i)

Impedance balance is defined as the ratio (expressed in dB) of common mode incident power at a 100 ohm impedance level to differential mode reflected power at a 25 ohm impedance level. The impedance balance is a bound on the coupling between common and differential modes.

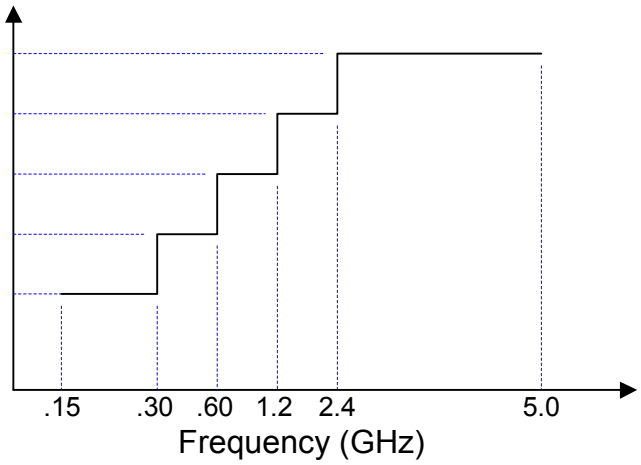


Figure 17: Impedance Balance Limits

6.2.2.3 Transmitted Signal Requirements Details

This section contains the details on Table 4 entries.

6.2.2.3.1 TX Differential Output Voltage

The differential voltage [(TX+) – (TX-)] measured at the Transmitter shall comply to the respective electrical specifications of section 6.2.

This is measured at mated Serial ATA connector on transmit side including any pre-emphasis.

6.2.2.3.2 TX Minimum Voltage Measurement Interval

The point within a UI where the signal shall meet minimum levels.

6.2.2.3.3 TX Rise/Fall Time

Rise times and fall times are measured between 20% and 80% of the signal, see Figure 18. The Rise and fall time requirement $t_{r/f}$ applies to differential transitions (TX+ – TX-), for both In-Band and Out-Of-Band signaling.

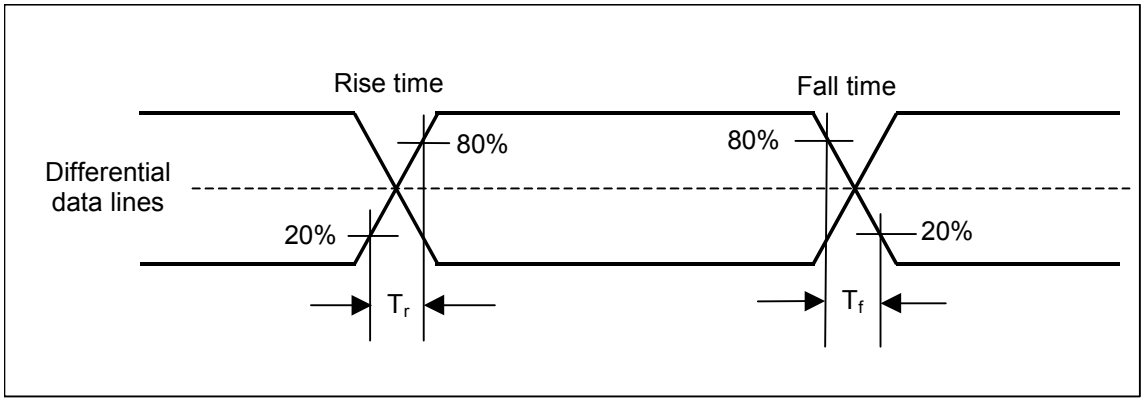


Figure 18: Signal rise and fall times

6.2.2.3.4 TX Differential Skew (Gen2i, Gen1x, Gen2x)

TX Differential Skew is the time difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX- signal falling/rising edge. It is an important parameter to control as excessive skew can result in increased high frequency jitter and common mode noise levels seen at the far end of the interconnect. The effects on the receiver are addressed in more detail in section 6.2.2.5.4. Excessive TX Differential Skew also increases EMI emissions.

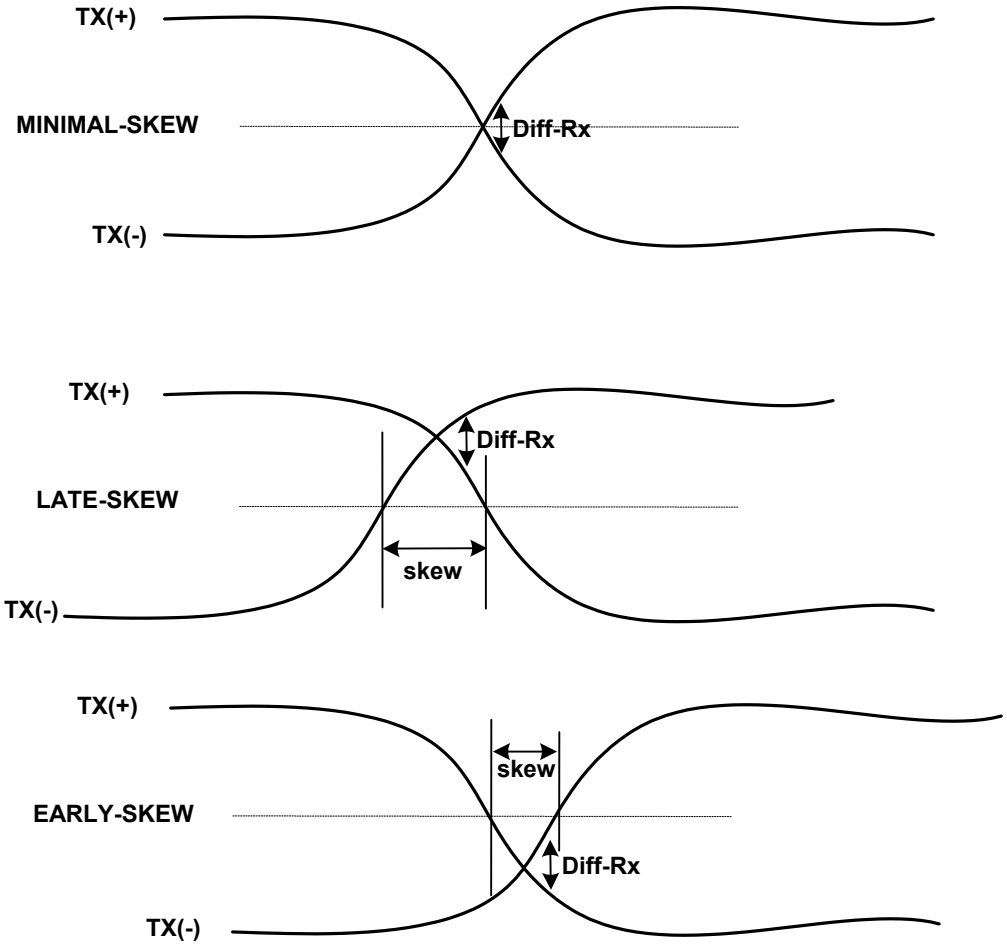


Figure 19: TX Intra-pair Skew

6.2.2.3.5 TX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)

Maximum sinusoidal amplitude of common mode signal measured at the transmitter connector.

The Transmitter shall comply to the electrical specifications of section 6.2, when subjected to a sinusoidal interfering signal with peak-to-peak voltage, and swept from the frequency range extremes, at a sweep rate period no shorter than 33.33 us.

6.2.2.3.6 Common Mode Transient Settle Time (Gen1i)

In Gen1i AC-coupled transmitters, this is the maximum time for common-mode transients to settle to within 10% of their actual operating $V_{CM,DC}$ value during transitions to and from the Idle Bus Condition.

6.2.2.3.7 OOB Differential Delta (Gen2i, Gen1x, Gen2x)

The difference between the average differential value during the idle bus condition and the average differential value during burst on transitions to and from the idle bus condition.

During OOB transmission, imperfections and asymmetries in transmitters can generate error signals that impair proper detection by a receiver. The OOB Differential Delta describes an error from the difference in transmitter DC offset during the idle and active conditions. Since the transmitter is alternating between idle and active conditions each with different DC offsets, an AC error voltage is generated which is a square wave at about 1 / (2*106nS) = 4.7MHz. The AC error voltage propagates through the interconnect and causes an offset in the receiver OOB detector.

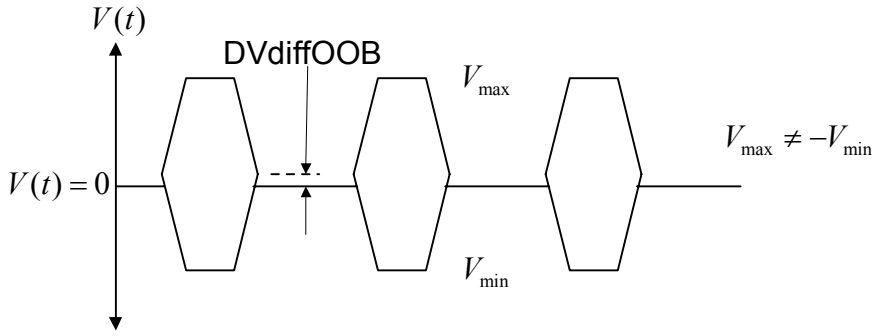


Figure 20: OOB Differential Delta (at Compliance Point with AC coupling)

6.2.2.3.8 OOB Common Mode Delta (Gen2i, Gen1x, Gen2x)

The difference between the common mode value during the idle bus condition and the common mode value during a burst on transitions to and from the idle bus condition.

6.2.2.3.9 TX Rise/Fall Imbalance

The match in the rise of TX+ and fall of TX- determined by the functions: absolute value(TX+,rise – TX-,fall)/average where average is (TX+,rise + TX-,fall)/2 and all rise and fall times are 20-80%.
The match in the fall of TX+ and rise of TX- determined by the function: absolute value(TX+,fall – TX-,rise)/average where average is (TX+,fall + TX-,rise)/2 and all rise and fall times are 20-80%.

6.2.2.3.10 TX Amplitude Imbalance (Gen2i, Gen1x, Gen2x)

The match in the amplitudes of TX+ and TX- determined by the function: absolute value(TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2 and all amplitudes are determined by mode (most prevalent) voltage.

6.2.2.3.11 Data-to-Data Transmit Jitter (Gen1i)

The Serial ATA interface jitter characteristics shall comply to within the jitter budget allocations in Table 3. This does not include UI error due to frequency skew (XTAL or SSC related).

Data-to-Data jitter requirements only apply to Gen1i. Data-to-Data jitter is a measure of variance in the zero crossing times of edges at a fixed time (t_n) equal to an integer number of Unit intervals (n) after triggering on data edges (t_0). Since t_0 is triggered from the serial signal rather than a Reference Clock the resulting measurements do represent a combination of the jitter at t_0 and t_n.

6.2.2.3.12 Clock-to-Data Transmit Jitter (Gen2i, Gen1x, Gen2x)

Gen1x, Gen2i, and Gen2x use a Clock-to-Data jitter requirement. Transmitters shall meet the jitter specifications for both tracking PLL frequency corners. Table 4 shows the maximum amount of jitter that a transmitter can generate and still be SATA compliant and section 6.4.8 describes the measurement. Since this specification places the compliance point at the connector, any jitter generated at the package connection, on the printed circuit board, and at the board connector shall be included in the measurement.

6.2.2.4 Receiver Specification Details

This section contains the details on Table 5 entries.

6.2.2.4.1 RX Pair Differential Impedance (Gen1i)

As seen by a differential TDR with 100 ps (max) edge looking into connector (20%-80%). Measured with TDR in differential mode.

6.2.2.4.2 RX Single-Ended Impedance (Gen1i)

As seen by TDR with 100 ps (max) edge looking into connector (20%-80%).

TDR set to produce simultaneous positive pulses on both signals of the RX pair. Single-ended impedance is the resulting (even mode) impedance of each signal. Both signals shall meet the single ended impedance requirement.

This requirement shall be met during all possible power and electrical conditions of the PHY including power off and power ramping.

6.2.2.4.3 RX Differential Mode Return Loss (Gen2i)

See details in section 6.2.2.2.1.

6.2.2.4.4 RX Common Mode Return Loss (Gen2i)

See details in section 6.2.2.2.4

6.2.2.4.5 RX Impedance Balance (Gen2i)

See details in section 6.2.2.2.5

6.2.2.5 Lab-Sourced Signal Details

This section contains the details on Table 6 entries.

The Lab-Sourced signal is a laboratory generated signal which is calibrated into a Laboratory Load and then applied to the RX+ and RX- signals of the Receiver Under Test. During calibration, the characteristics of the Lab-Sourced signal shall comply with the specifications of Table 6. When this signal is then applied to the Receiver Under Test the Frame Error Rate specifications of Table 2 shall be met.

6.2.2.5.1 RX Differential Input Voltage

The RX Differential Input Voltage is the range of input voltage under compliance test conditions that a receiver shall operate to the required link performance level. This is one range of input conditions a receiver shall tolerate (see section 6.4.9).

The Serial ATA system has a transmitter and receiver with impedances near the nominal system impedance of 100 ohms. The voltage at compliance points is strongly dependent on the transmitter, receiver, and interconnect impedances. The RX differential input voltage is delivered from an impedance matched signal source into a matched load (see Figure 21). When the actual receiver is substituted for the matched load, the voltage changes by an amount that is receiver design dependent. This change is part of the receiver design burden.

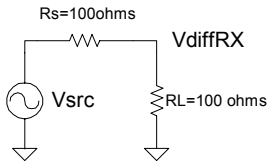


Figure 21: RX Differential Input Voltage Conditions

The RX differential input voltage DOES NOT describe the voltage delivered from interconnect. The interconnect output impedance is not equal to the nominal system impedance over the entire frequency range. It is NOT the voltage at a matched load delivered from interconnect, NOR is it the voltage at a receiver delivered from interconnect. Example calculations demonstrating this are given in section 6.4.4.

6.2.2.5.2 RX Rise/Fall Times

Rise times and fall times are measured between 20% and 80% of the signal The rise and fall time requirement $t_{20\text{-}80RX}$ applies to differential transitions (applied to RX+ and RX-).

6.2.2.5.3 RX Minimum Voltage Measurement Interval

The point in a UI that the signal shall meet minimum levels.

6.2.2.5.4 RX Differential Skew (Gen2i, Gen1x, Gen2x)

RX Differential Skew is the time difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX- signal falling/rising edge, as measured at the RX connector. The receiver should tolerate the RX skew levels per Table 6, as generated by a Lab-Sourced Signal.

The receiver differential skew is an important parameter to consider, as excessive skew can result in increased high frequency jitter and high frequency common mode noise seen at the high-speed differential receiver. Figure 22 depicts how late and early skew signaling affect the time at which the differential receiver resolves the differential input signals. For the minimal skew case, when the single-ended slew rate is maximum at the crossover, the UI width is maximized. However, this is not the case for the early and late skew cases. The high frequency common mode noise is a result of the rapid changing of the operating point of the high speed receiver. Section 6.4.12 describes the applicable measurement method that can be used to calibrate the intentionally skewed Lab-Sourced Signal output into the receiver.

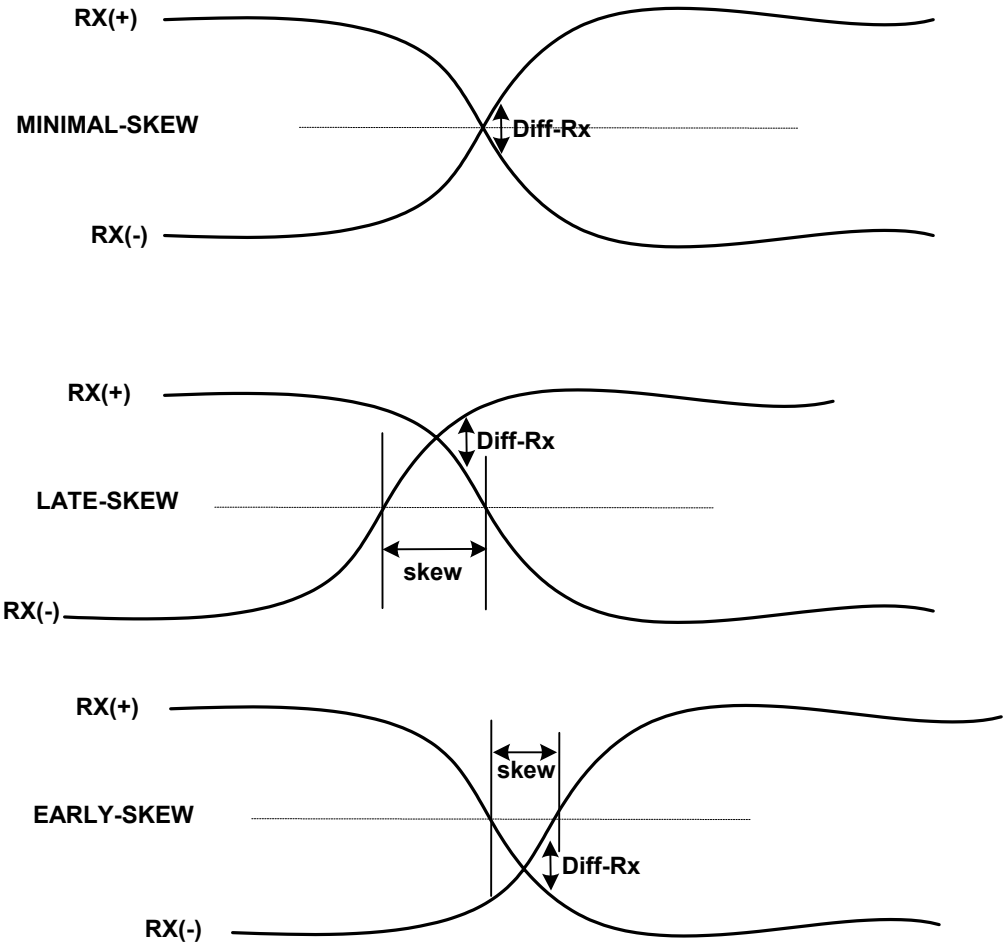


Figure 22: RX Intra-pair Skew

6.2.2.5.5 RX AC Common Mode Voltage (Gen2i, Gen1x, Gen2x)

Max peak-to-peak sinusoidal amplitude of ac common mode signal [(RX+) + (RX-)]/2.

The Receiver shall operate to within the frame error rate cited in Table 2, when subjected to a sinusoidal common mode interfering signal with peak-to-peak voltage $V_{cmRX,ac}$ defined in Table 6 and swept across the frequency range, $f_{cm,acRX}$, defined in Table 6 at a sweep rate period no shorter than 33.33 us.

6.2.2.5.6 AC Common Mode Frequency

All receivers shall be able to tolerate sinusoidal common-mode noise components inside this frequency range with an amplitude of $V_{cm,acRX}$.

6.2.2.5.7 Data-Data Receiver Jitter Tolerance (Gen1i)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 6 and section 6.4.9 describes the measurement. Receivers shall tolerate jitter at the maximum levels specified for all UI spacings.

6.2.2.5.8 Clock-Data Receiver Jitter Tolerance (Gen2i, Gen1x, Gen2x)

Jitter tolerance is the ability of the receiver to recover data in the presence of jitter. The minimum amount of jitter that a receiver shall be able to operate is the jitter tolerance specification provided in Table 6 and section 6.4.9 describes the measurement. Receivers shall tolerate at least the jitter for both corner frequencies listed.

6.2.2.6 OOB Specifications Details

This section provides details on Table 7.

6.2.2.6.1 OOB Signal Detection Threshold

Differential signal amplitude detected as activity by the squelch detector during OOB signaling.

V_{diffRX} signals less than the minimum V_{thresh} defined in Table 7 shall not be detected as activity. Signal levels greater than the maximum V_{thresh} defined in Table 7 shall be detected as activity.

6.2.2.6.2 UI during OOB Signaling

Operating data period during OOB burst transmission (at Gen1 rate +/- 3%).

6.2.2.6.3 COMINIT/RESET and COMWAKE Transmit Burst Length

Burst length in terms of UI_{OOB} as measured from 100mV differential crosspoints of first and last edges of a burst.

6.2.2.6.4 COMINT/RESET Transmit Gap Length

Gap length in terms of UI_{OOB} as measured from 100mV differential crosspoints of last and first edges of bursts.

6.2.2.6.5 COMWAKE Transmit Gap Length

Gap length in terms of UI_{OOB} as measured from 100mV differential crosspoints of last and first edges of bursts.

6.2.2.6.6 COMWAKE Gap Detection Windows

Three timing ranges defining the validation and invalidation of COMWAKE gaps, see Table 7.

Any OOB gap between bursts falling in the defined “May detect” range may be recognized as a valid COMWAKE gap.

Any OOB gap between bursts falling in the “Shall detect” range shall be recognized as a valid COMWAKE gap.

Any OOB gap between bursts falling in the “shall not detect” ranges shall be recognized as an invalid COMWAKE gap (shall not be recognized as a valid COMWAKE gap).

6.2.2.6.7 COMINIT/RESET Gap Detection Windows

Three timing ranges defining the validation and invalidation of COMINIT and COMREST gaps, see Table 7.

Any OOB gap between bursts falling in the defined “May detect” range may be recognized as a valid COMINIT or COMREST gap.

Any OOB gap between bursts falling in the “Shall detect” range shall be recognized as a valid COMINIT or COMREST gap.

Any OOB gap between bursts falling in the “shall not detect” ranges shall be recognized as an invalid COMINIT or COMRESET gap (shall not be recognized as a valid COMINT or COMRESET gap).

6.2.3 Loopback

In addition to meeting all electrical specifications in Tables 2 through 7, all Hosts and Devices shall provide Far-End Retimed Loopback mode. Two other loopback modes are optional but if implemented shall comply with 6.2.3.2 and 6.2.3.3.

a) Far-End Retimed - Required
b) Far-End Analog - Optional
c) Near-End Analog (Effectively Retimed) - Optional

6.2.3.1 Loopback -- Far end retimed

Figure 23 below, illustrates the scope, at the architectural block diagram level, of the Far-End Retimed loopback. As this loopback scheme needs a specific action from the far-end connected interface, this mode shall be entered by way of the BIST FIS described in Serial ATA 1.0a.

The Far-End Interface shall remain in this Far-End Retimed Loopback, until receipt of the COMRESET/COMINIT OOB Signaling sequence.

As a minimum, Far-End Retimed Loopback shall involve far-end circuitry such that the data stream, at the Far-End interface, is extracted by the Deserializer and data recovery circuit (DRC) before being sent back through the Serializer and Transmitter with appropriately inserted retiming ALIGN primitives as described in section 6.5.3. The data may be decoded and descrambled in order to provide testing coverage for those portions of the device, provided the data is re-scrambled using the same sequence of scrambler syndromes. The returned data shall be the same as the received data with the exception that the returned data may be encoded with different starting running disparity.

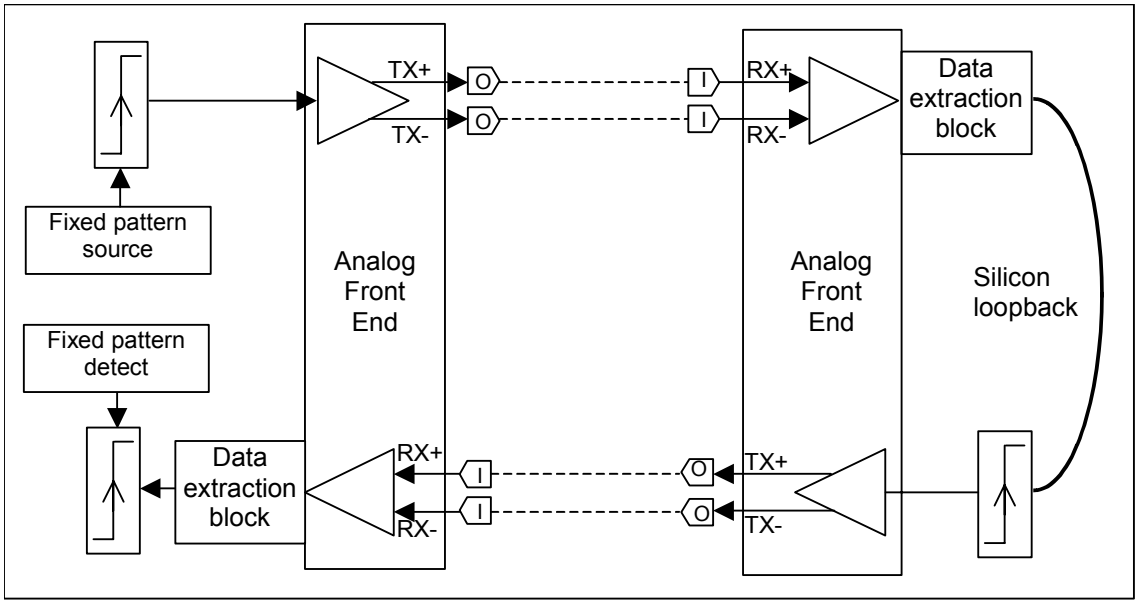


Figure 23: Loopback far-end retimed

6.2.3.2 Loopback - far end analog-[Optional]

This is an optional feature which if implemented shall be consistent with all requirements of this section. Figure 24 below, illustrates the scope, at the architectural block diagram level, of the Far-End Analog loopback. As this loopback scheme needs a specific action from the far-end connected interface, this mode shall be entered by way of the BIST FIS described in Serial ATA 1.0a.

The Far-End Interface shall remain in this Far-End Analog Loopback mode, until receipt of the COMRESET/COMINIT OOB Signaling sequence.

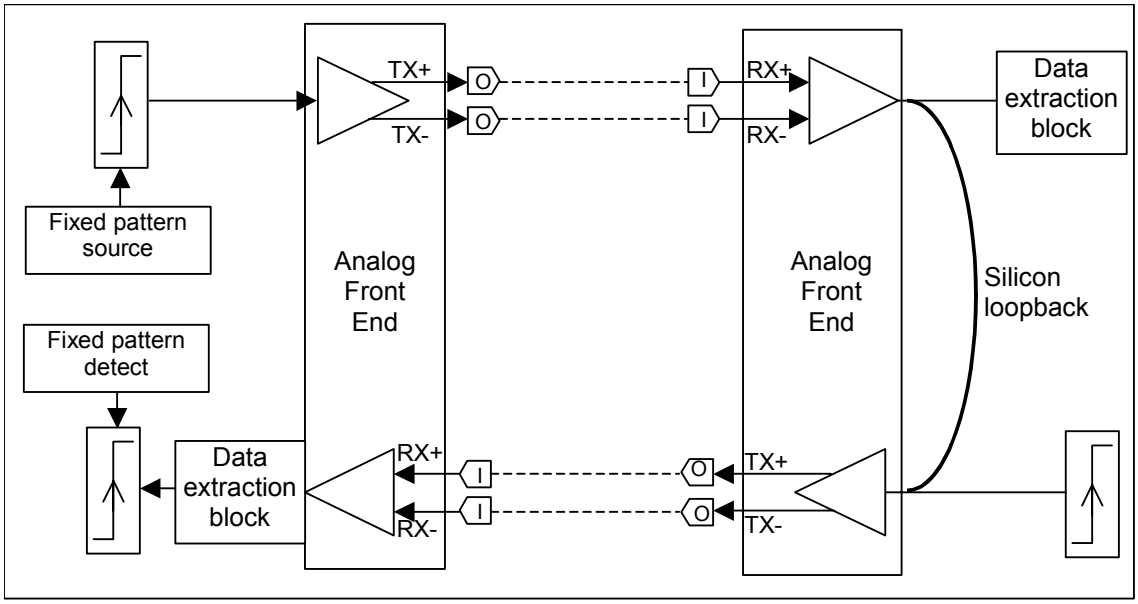


Figure 24: Loopback far-end analog

6.2.3.3 Loopback - near end analog-[Optional]

This is an optional feature. Figure 25 below, illustrates the scope, at the architectural block diagram level, of the Near-End Analog loopback. This loopback scheme, if implemented, needs the far-end connected interface to be in a non-transmitting mode, such as Slumber, or Partial interface power management states. Entry to and exit from this mode is vendor specific.

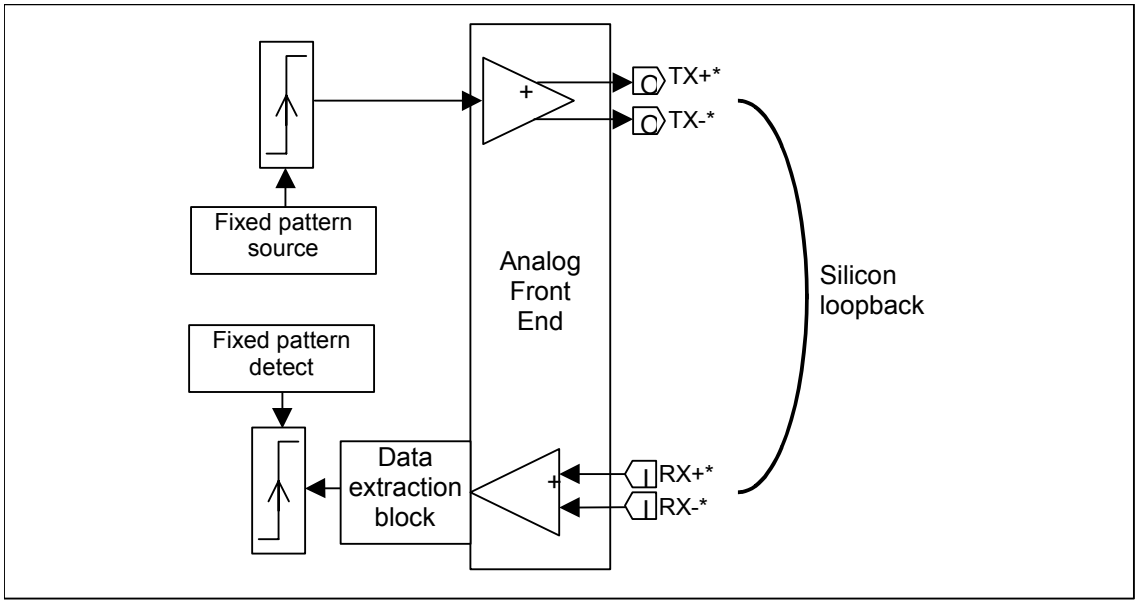


Figure 25: Loopback - near-end analog

6.2.4 Test Pattern Requirements

Test patterns shall be used for compliance testing of the Serial ATA interfaces. This section defines various patterns to be used in Compliance Testing. Individual sections within Section 6.4 define which patterns are to be used for specific tests. The patterns are classified in two categories:

a) Non-compliant patterns
b) Compliant patterns

Non-compliant patterns are those patterns that are used for baseline jitter measurements, and assessment of signal quality, given specified stimulus. These patterns do not comply to the required FIS formats, but are just a repeated selected set of 8b/10b characters.

Compliant patterns are those specified patterns that contain the leading SOF primitive, the specified pattern as data content, and trailing CRC, and EOF primitives. There is no suppression of the dual-consecutive ALIGN primitive during stimulus with this class of pattern.

Test patterns cited in this section used as stimulus that will be used to verify the Serial ATA interface compliance and signal integrity, using the following test models:

a) Non-compliant test patterns for jitter measurements, physical connection media tests, and electrical parameter testing.
b) Compliant test patterns for frame error rate testing and in-system tests.

6.2.4.1 Test requirements - non-compliant patterns

Electrical parameters of section 6.2 shall be verified using the following set of test patterns, using the BIST FIS, Far-End Transmit Mode.

a) Low transition density bit patterns, as per section 6.2.4.3.1.
b) High transition density bit patterns as per section 6.2.4.3.2.
c) Low frequency spectral component bit patterns as per section 6.2.4.3.3.
d) Simultaneous switching outputs bit patterns as per section 6.2.4.3.4
e) Lone bit patterns as per section 6.2.4.3.5.

6.2.4.2 Test requirements - compliant frame patterns

The frame error rates specified in section 6.4.1.2 shall be tested for compliance when subjected to any implementation-determined worst-case compliant patterns, as well as the following set of compliant patterns:

a) Compliant low transition density bit patterns, as per section 6.2.4.3.1.
b) Compliant high transition density bit patterns as per section 6.2.4.3.2.
c) Compliant low frequency spectral component bit patterns as per section 6.2.4.3.3.
d) Compliant simultaneous switching outputs bit patterns as per section 6.2.4.3.4.
e) Compliant lone bit patterns as per section 6.2.4.3.5.
f) Compliant composite patterns as per section 6.2.4.3.6.

Where the qualifying prefix term "compliant" signifies transmission of the cited pattern encapsulated in the data portion of the Frame Information Structure, and used in a Serial ATA operational transmission context.

Note that the cited patterns should appear on the wire, and the N parameters of the reference patterns shall be extended to achieve the maximum frame length. These compliant patterns contain the necessary SOF leading primitive, the calculated CRC, and the trailing EOF primitive, as shown in Figure 26 below. Note that encoding and scrambling determine the data patterns on the wire. The burden is upon the reader to generate these patterns consistently with this specification.

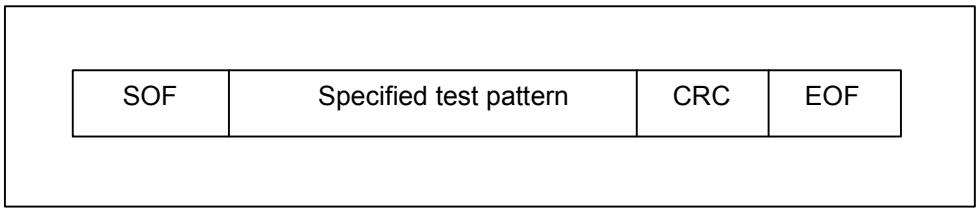


Figure 26: Compliant test patterns

6.2.4.3 Test bit patterns and sequence characteristics

There are various types of bit sequence patterns that emphasize low/high transition density patterns, as well as low/high frequency patterns.

a) Low transition density patterns are those patterns containing long runs of ones and zeroes, intended to create inter-symbol interference by varying the excursion times at either extreme of the differential signaling levels.

b) High transition density patterns are those patterns containing short runs of ones and zeroes, also intended to create inter-symbol interference.

c) Bit patterns that contain low frequency spectral components are a good test of the input high pass filter circuitry, more specifically, introduced amplitude signal distortion, due to a marginal design. These bit patterns are a better test than those bit patterns having high frequency spectral content.

d) Simultaneous switching outputs patterns are achieved by transmitting alternating 1's complement bit patterns (10-bits) for recovery at the receiver. These patterns create worst case power supply, or chip substrate, noise, and are achieved by selecting bit test pattern sequences that maximize current extremes at the recovered bit pattern parallel interface. These patterns induce Ldi/dt noise into substrate supply, and are a good test of the receiver circuitry.

e) The Lone-bit patterns are comprised of the consecutive combination of certain 10b patterns that result in a lone-bit. More specifically, a lone-bit is prefixed by a run-length of four bits and followed by a run-length of three. These patterns create a condition where the preceding 4-bit run-length results in minimum amplitude of the lone-bit as well as its time-width in comparison to its surrounding segments. This is often the worst case condition that the receiving data recovery circuits will encounter.

f) The intent of random bit patterns is to provide those patterns containing sufficiently broad spectral content, and minimal peaking, that can be used for both component, and system level architecture measurement of jitter output, and bit-error-rate performance. These patterns are also intended to be the common baseline pattern stimulus, for system/component vendor comparative testing, attributing the Transmit jitter output measurement to the component performance, and not to the spectral profile of the data pattern used.

The test patterns illustrated in the following sections are indicated to start with negative running disparity for illustrative purposes only in order to convey the encoded 10b patterns transmitted for each sequence.

6.2.4.3.1 Low Transition Density Patterns (LTDP)

Low transition density bit patterns (LTDP), as shown in Figure 27 and Figure 28 below, contain long runs of ones and zeroes. These patterns create jitter due to inter-symbol interference. This is aggravated when part of the composite pattern described in section 6.2.4.3.6. Bit sequences are shown for both cases, where the starting running disparity is negative or positive.

LTDP Starting with RD-

Transmission order →

-	D17.7(F1h)-		D30.7(FEh)+			D7.1(27h)+			D14.7(EEh)+		-
	1000	1101	1110	0001	1110	0001	1110	0101	1100	1000	
	8	D	E	1	E	1	E	5	C	8	
-	D30.7(FEh)-		D7.6(C7h)-			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	0111	1000	0110	0111	1000	1110	0001	1100	
	7	8	7	8	6	7	8	E	1	C	
-	D30.3(7Eh)-		D30.3(7Eh)+			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	1110	0001	1100	0111	1000	1110	0001	1100	
	7	8	E	1	C	7	8	E	1	C	
	Above Dword is repeated a total of 2045 times for long version **Above Dword is repeated a total of 125 times for short version**										
-	D3.7(E3h)-		D28.7(FCh)+			D3.7(E3h)-			D28.7(FCh)+		-
	1100	0111	1000	1110	0001	1100	0111	1000	1110	0001	
	C	7	8	E	1	C	7	8	E	1	

Figure 27: Low Transition Density Pattern (LTDP) starting with RD-

Long version total: 3 + 2045 = 2048 Dwords
Short version total: 3 + 125 = 128 Dwords

LTDP Starting with RD+
Transmission order

+	D14.7(EEh)+		D30.7(FEh)-			D7.6(C7h)+			D17.7(F1h)-		+
	0111	0010	0001	1110	0001	1110	0001	1010	0011	0111	
	7	2	1	E	1	E	1	A	3	7	
+	D30.7(FEh)+		D7.1(27h)+			D30.3(7Eh)+			D30.3(7Eh)-		+
	1000	0111	1000	0111	1001	1000	0111	0001	1110	0011	
	8	7	8	7	9	8	7	1	E	3	
+	D30.3(7Eh)+		D30.3(7Eh)-			D30.3(7Eh)+			D30.3(7Eh)-		+
	1000	0111	0001	1110	0011	1000	0111	0001	1110	0011	
	8	7	1	E	3	8	7	1	E	3	
	Above Dword is repeated a total of 2045 times for long version **Above Dword is repeated a total of 125 times for short version**										
+	D28.7(FCh)+		D3.7(E3h)-			D28.7(FCh)+			D3.7(E3h)-		+
	0011	1000	0111	0001	1110	0011	1000	0111	0001	1110	
	3	8	7	1	E	3	8	7	1	E	

Figure 28: Low Transition Density Pattern (LTDP) starting with RD+

Long version total: 3 + 2045 = 2048 Dwords
Short version total: 3 + 125 = 128 Dwords

6.2.4.3.2 High Transition Density Patterns (HTDP)

High transition density patterns are those patterns containing short runs of ones and zeroes, as shown in Figure 29 and Figure 30 below. These patterns create jitter due to inter-symbol interference, becoming more pronounced when part of the composite pattern described in section 6.2.4.3.6. There are two types of high-transition density patterns of interest:

a) Half-rate high transition density bit pattern sequence
b) Quarter-rate high transition density bit pattern sequence

Both types are used in the high transition density test pattern. Bit sequences are shown for both cases, where the starting running disparity is negative or positive.

HTDP Starting with –RD+

Transmission order →

-	D21.5(B5h)-				D21.5(B5h)-				D21.5(B5h)-				D21.5(B5h)-				-
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010							
	A	A	A	A	A	A	A	A	A	A							

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

-	D24.3(78h)-				D24.3(78h)+				D24.3(78h)-				D24.3(78h)+				-
	1100	1100	1100	1100	1100	1100	1100	1100	1100	1100							
	C	C	C	C	C	C	C	C	C	C							

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

-	D10.2(4Ah)-				D10.2(4Ah)-				D10.2(4Ah)-				D10.2(4Ah)-				-
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101							
	5	5	5	5	5	5	5	5	5	5							

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

-	D25.6(D9h)-				D6.1(26h)+				D25.6(D9h)-				D6.1(26h)+				-
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001							
	9	9	9	9	9	9	9	9	9	9							

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

Figure 29: High Transition Density Pattern (HTDP) starting with RD-

Long version total: 4 * 512 = 2048 Dwords
Short version total: 4 * 32 = 128 Dwords

HTDP Starting with RD+

Transmission order →

+	D21.5(B5h)+		D21.5(B5h)+		D21.5(B5h)+		D21.5(B5h)+				+
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

+	D24.3(78h)+		D24.3(78h)+		D24.3(78h)+		D24.3(78h)+				+
	0011	0011	0011	0011	0011	0011	0011	0011	0011	0011	
	3	3	3	3	3	3	3	3	3	3	

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

+	D10.2(4Ah)+		D10.2(4Ah)+		D10.2(4Ah)+		D10.2(4Ah)+				+
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

+	D25.6(D9h)+		D6.1(26h)+		D25.6(D9h)+		D6.1(26h)+				+
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	

Above Dword is repeated a total of 512 times for long version
Above Dword is repeated a total of 32 times for short version

Figure 30: High Transition Density Pattern (HTDP) starting with RD+

Long version total: 4 * 512 = 2048 Dwords
Short version total: 4 * 32 = 128 Dwords

6.2.4.3.3 Low Frequency Spectral Content Pattern (LFSCP)

Bit patterns that contain low frequency spectral components, as shown in Figure 31 and Figure 32 below, are a good test of the interconnect transmission, especially any AC coupling capacitors. Poor transmission through these components introduces signal distortion shown by this test pattern. Bit sequences are shown for both cases, where the starting running disparity is negative or positive.

LFSCP Starting with –RD-

Transmission order →

-	D20.2(54h)-		D20.2(54h)-			D20.2(54h)-		D20.2(54h)-			-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	
	2	D	4	B	5	2	D	4	B	5	
	Above Dword is repeated a total of 1023 times for long version **Above Dword is repeated a total of 63 times for short version**										
-	D20.2(54h)-		D20.7(F4h)-			D11.5(ABh)+		D11.5(ABh)+			+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	
	2	D	4	B	7	D	2	B	4	A	
+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+		D11.5(ABh)+			+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	D	2	B	4	A	D	2	B	4	A	
	Above Dword is repeated a total of 1023 times for long version **Above Dword is repeated a total of 63 times for short version**										
+	D11.5(ABh)+		D11.7(EBh)+			D20.2.(54h)-		D20.2(54h)-			-
	1101	0010	1011	0100	1000	0010	1101	0100	1011	0101	
	D	2	B	4	8	2	D	4	B	5	

Figure 31: Low Frequency Spectral Content Pattern (LFSCP) starting with RD-

Long version total: 2 + 2 * 1023 = 2048 Dwords
4095 bytes of D11.5, 4095 bytes of D20.2
1 D11.7 transitional byte including 0000010 run, 1 D20.7 transitional byte including 1111101 run

Short version total: 2 + 2 * 63 = 128 Dwords
255 bytes of D11.5, 255 bytes of D20.2
1 D11.7 transitional byte including 0000010 run, 1 D20.7 transitional byte including 1111101 run

LFSCP Starting with RD+

Transmission order →

+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+		D11.5(ABh)+		+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010
	D	2	B	4	A	D	2	B	4	A

Above Dword is repeated a total of 1023 times
Above Dword is repeated a total of 63 times for short version

+	D11.5(ABh)+		D11.7(EBh)+			D20.2.(54h)-		D20.2(54h)-		-
	1101	0010	1011	0100	1000	0010	1101	0100	1011	0101
	D	2	B	4	8	2	D	4	B	5

-	D20.2(54h)-		D20.2(54h)-			D20.2(54h)-		D20.2(54h)-		-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101
	2	D	4	B	5	2	D	4	B	5

Above Dword is repeated a total of 1023 times
Above Dword is repeated a total of 63 times for short version

-	D20.2(54h)-		D20.7(F4h)-			D11.5(ABh)+		D11.5(ABh)+		+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010
	2	D	4	B	7	D	2	B	4	A

Figure 32: Low Frequency Spectral Content Pattern (LFSCP) starting with RD+

Long version total: 2 + 2 * 1023 = 2048 Dwords
4095 bytes of D11.5, 4095 bytes of D20.2
1 D11.7 transitional byte including 0000010 run, 1 D20.7 transitional byte including 1111101 run

Short version total: 2 + 2 * 63 = 128 Dwords
255 bytes of D11.5, 255 bytes of D20.2

6.2.4.3.4 Simultaneous Switching Outputs Pattern (SSOP)

The Simultaneous switching outputs bit pattern (SSOP), shown in Figure 33 and Figure 34 below, induces inductive switching (Ldi/dt) noise into substrate supply of a receiver providing a good test of noise control. The SSOP pattern, alternating 1's complement bit patterns (10-bits), are applied to a receiver. Bit sequences are shown for both cases, where the starting running disparity is negative or positive.

SSOP Starting with –RD-
Transmission order →

-	D31.3(7Fh)-		D31.3(7Fh)+			D31.3(7Fh)-			D31.3(7Fh)+		-
	1010	1100	1101	0100	1100	1010	1100	1101	0100	1100	
	A	C	D	4	C	A	C	D	4	C	

Above Dword is repeated a total of 2048 times for long version
Above Dword is repeated a total of 128 times for short version

Figure 33: Simultaneous Switching Outputs Pattern (SSOP) starting with RD-

Long version total: 1 * 2048 = 2048 Dwords
Short version total: 1 * 128 = 128 Dwords

SSOP Starting with RD+
Transmission order →

+	D31.3(7Fh)+		D31.3(7Fh)-			D31.3(7Fh)+			D31.3(7Fh)-		+
	0101	0011	0010	1011	0011	0101	0011	0010	1011	0011	
	5	3	2	B	3	5	3	2	B	3	

Above Dword is repeated a total of 2048 times for long version
Above Dword is repeated a total of 128 times for short version

Figure 34: Simultaneous Switching Outputs Pattern (SSOP) starting with RD+

Long version total: 1 * 2048 = 2048 Dwords
Short version total: 1 * 128 = 128 Dwords

6.2.4.3.5 Lone-Bit Pattern (LBP)

The Lone-Bit Patterns, shown in Figure 35 and Figure 36 below, are comprised of the combination of adjacent 10B patterns, resulting in a Lone-bit prefixed by a run length of four, and suffixed by a run length of three. This is a good test of the receiver jitter tolerance under adverse signaling conditions. The lone-bit will be attenuated, and be narrower than expected. Bit sequences are shown for both cases, where the starting running disparity is negative or positive.

LBP Starting with –RD-
Transmission order →

-	D12.0(0Ch)-		D11.4(8Bh)+			D12.0(0Ch)-		D11.4(8Bh)+			-
	0011	0110	1111	0100	0010	0011	0110	1111	0100	0010	
	3	6	F	4	2	3	6	F	4	2	
	Above Dword is repeated a total of 2048 times for long version **Above Dword is repeated a total of 128 times for short version**										

Figure 35: Lone-Bit Pattern (LBP) starting with RD-

Long version total: 1 * 2048 = 2048 Dwords
Short version total: 1 * 128 = 128 Dwords

LBP Starting with RD+
Transmission order →

+	D11.4(8Bh)+		D12.0(0Ch)-			D11.4(8Bh)+		D12.0(0Ch)-			+
	1101	0000	1000	1101	1011	1101	0000	1000	1101	1011	
	D	0	8	D	B	D	0	8	D	B	
	Above Dword is repeated a total of 2048 times for long version **Above Dword is repeated a total of 128 times for short version**										

Figure 36: Lone-Bit Pattern (LBP) starting with RD+

Long version total: 1 * 2048 = 2048 Dwords
Short version total: 1 * 128 = 128 Dwords

NOTE: Care must be taken when generating the Lone Bit Pattern from 8B data. Two potential 8B patterns are available: 8B_0C_8B_0C if the initial Running Disparity is positive (RD+) or 0C_8B_0C_8B if the initial Running Disparity is negative (RD-). It is important that the selected 8B pattern match the initial running disparity or else the 10B pattern will not match the Lone Bit Pattern. For example, if 8B_0C_8B_0C is transmitted when the initial Running Disparity is negative, the 10B data will not match the 10B data of the Lone Bit Pattern. A similar mismatch will occur if the 0C_8B_0C_8B pattern is transmitted when the initial Running Disparity is positive.

6.2.4.3.6 Composite Pattern (COMP)

For the measurement of jitter, the Composite patterns, as shown in Figure 37 and Figure 38 below, should combine low frequency, low transition density, and high transition density patterns. All these combinations, but the Low Frequency Spectral Content class can be performed for relatively short test time intervals, for good jitter performance measurements.

The lower frequency pattern needs to be tested for longer interval periods to be able to observe the lower frequency jitter effects on the interface.

The composite pattern (COMP) stresses the interface components within the link with low and high frequency jitter, tests for component, and various amplitude distortions due to marginal receiver input circuitry, or interface components.

Note that for the sequence that totals only 128 Dwords, the 128-Dword composite pattern is too short to get a sufficient number of continuous repeats for each pattern type.

Composite Pattern Starting with RD-

Transmission order →

-	D31.3(7Fh)-		D31.3(7Fh)+			D31.3(7Fh)-		D31.3(7Fh)+			-
	1010	1100	1101	0100	1100	1010	1100	1101	0100	1100	
	A	C	D	4	C	A	C	D	4	C	

Above Dword is repeated a total of 256 times for long version
Above Dword is repeated a total of 16 times for short version

-	D21.5(B5h)-		D21.5(B5h)-			D21.5(B5h)-		D21.5(B5h)-			-
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

-	D24.3(78h)-		D24.3(78h)+			D24.3(78h)-		D24.3(78h)+			-
	1100	1100	1100	1100	1100	1100	1100	1100	1100	1100	
	C	C	C	C	C	C	C	C	C	C	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

-	D10.2(4Ah)-		D10.2(4Ah)-			D10.2(4Ah)-		D10.2(4Ah)-			-
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

-	D25.6(D9h)-		D6.1(26h)+			D25.6(D9h)-		D6.1(26h)+			-
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

-	D17.7(F1h)-		D30.7(FEh)+			D7.1(27h)+			D14.7(EEh)+		-
	1000	1101	1110	0001	1110	0001	1110	0101	1100	1000	
	8	D	E	1	E	1	E	5	C	8	

-	D30.7(FEh)-		D7.6(C7h)-			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	0111	1000	0110	0111	1000	1110	0001	1100	
	7	8	7	8	6	7	8	E	1	C	

-	D30.3(7Eh)-		D30.3(7Eh)+			D30.3(7Eh)-			D30.3(7Eh)+		-
	0111	1000	1110	0001	1100	0111	1000	1110	0001	1100	
	7	8	E	1	C	7	8	E	1	C	

Above Dword is repeated a total of 509 times for long version
Above Dword is repeated a total of 29 times for short version

-	D3.7(E3h)-		D28.7(FCh)+			D3.7(E3h)-			D28.7(FCh)+		-
	1100	0111	1000	1110	0001	1100	0111	1000	1110	0001	
	C	7	8	E	1	C	7	8	E	1	

-	D12.0(0Ch)-		D11.4(8Bh)+			D12.0(0Ch)-			D11.4(8Bh)+		-
	0011	0110	1111	0100	0010	0011	0110	1111	0100	0010	
	3	6	F	4	2	3	6	F	4	2	

Above Dword is repeated a total of 256 times for long version
Above Dword is repeated a total of 16 times for short version

-	D20.2(54h)-		D20.2(54h)-			D20.2(54h)-			D20.2(54h)-		-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	
	2	D	4	B	5	2	D	4	B	5	

Above Dword is repeated a total of 255 times for long version
Above Dword is repeated a total of 15 times for short version

-	D20.2(54h)-		D20.7(F4h)-			D11.5(ABh)+			D11.5(ABh)+		+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	
	2	D	4	B	7	D	2	B	4	A	

+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+			D11.5(ABh)+		+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	D	2	B	4	A	D	2	B	4	A	

Above Dword is repeated a total of 255 times for long version
Above Dword is repeated a total of 15 times for short version

+	D11.5(ABh)+		D11.7(EBh)+			D20.2.(54h)-			D20.2.(54h)-		-
	1101	0010	1011	0100	1000	0010	1101	0100	1011	0101	
	D	2	B	4	8	2	D	4	B	5	

-	D21.5(B5h)-		D21.5(B5h)-			D21.5(B5h)-			D21.5(B5h)-		-
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	

	A	A	A	A	A	A	A	A	A	A	
	Above Dword is repeated a total of 64 times for long version Above Dword is repeated a total of 4 times for short version										
	D24.3(78h)-		D24.3(78h)-		D24.3(78h)-		D24.3(78h)-				-
-	1100	1100	1100	1100	1100	1100	1100	1100	1100	1100	
	C	C	C	C	C	C	C	C	C	C	
	Above Dword is repeated a total of 64 times for long version Above Dword is repeated a total of 4 times for short version										
	D10.2(4Ah)-		D10.2(4Ah)-		D10.2(4Ah)-		D10.2(4Ah)-				-
-	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	
	Above Dword is repeated a total of 64 times for long version Above Dword is repeated a total of 4 times for short version										
	D25.6(D9h)-		D6.1(26h)+		D25.6(D9h)-		D6.1(26h)+				-
-	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	
	Above Dword is repeated a total of 64 times for long version Above Dword is repeated a total of 4 times for short version										

Figure 37: Composite-Bit Pattern (COMP) starting with RD-

Long version total: 2048 Dwords total
256DW SSOP
256DW HTDP (64DW, 64DW, 64DW, 64DW)
512DW LTDP (1DW, 1DW, 509DW, 1DW)
256DW LBP
512DW LFSCP (255DW, 1DW, 255DW, 1DW)
256DW HTDP (64DW, 64DW, 64DW, 64DW)

Short version total: 128 Dwords total
16DW SSOP
16DW HTDP (4DW, 4DW, 4DW, 4DW)
32DW LTDP (1DW, 1DW, 29DW, 1DW)
16DW LBP
32DW LFSCP (15DW, 1DW, 15DW, 1DW)
16DW HTDP (4DW, 4DW, 4DW, 4DW)

Composite Pattern Starting with RD+

Transmission order →

+	D31.3(7Fh)+		D31.3(7Fh)-			D31.3(7Fh)+		D31.3(7Fh)-			+
	0101	0011	0010	1011	0011	0101	0011	0010	1011	0011	
	5	3	2	B	3	5	3	2	B	3	

Above Dword is repeated a total of 256 times for long version
Above Dword is repeated a total of 16 times for short version

+	D21.5(B5h)+		D21.5(B5h)+			D21.5(B5h)+		D21.5(B5h)+			+
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D24.3(78h)+		D24.3(78h)+			D24.3(78h)+		D24.3(78h)+			+
	0011	0011	0011	0011	0011	0011	0011	0011	0011	0011	
	3	3	3	3	3	3	3	3	3	3	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D10.2(4Ah)+		D10.2(4Ah)+			D10.2(4Ah)+		D10.2(4Ah)+			+
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D25.6(D9h)+		D6.1(26h)+			D25.6(D9h)+		D6.1(26h)+			+
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D14.7(EEh)+		D30.7(FEh)-			D7.6(C7h)+		D17.7(F1h)-			+
	0111	0010	0001	1110	0001	1110	0001	1010	0011	0111	
	7	2	1	E	1	E	1	A	3	7	

+	D30.7(FEh)+		D7.1(27h)+			D30.3(7Eh)+		D30.3(7Eh)-			+
	1000	0111	1000	0111	1001	1000	0111	0001	1110	0011	
	8	7	8	7	9	8	7	1	E	3	

+	D30.3(7Eh)+		D30.3(7Eh)-			D30.3(7Eh)+		D30.3(7Eh)-			+
	1000	0111	0001	1110	0011	1000	0111	0001	1110	0011	
	8	7	1	E	3	8	7	1	E	3	

Above Dword is repeated a total of 509 times for long version
Above Dword is repeated a total of 29 times for short version

+	D28.7(FCh)+	D3.7(E3h)-	D28.7(FCh)+	D3.7(E3h)-	+

	0011	1000	0111	0001	1110	0011	1000	0111	0001	1110	
	3	8	7	1	E	3	8	7	1	E	

+	D11.4(8Bh)+		D12.0(0Ch)-			D11.4(8Bh)+		D12.0(0Ch)-			+
	1101	0000	1000	1101	1011	1101	0000	1000	1101	1011	
	D	0	8	D	B	D	0	8	D	B	

Above Dword is repeated a total of 256 times for long version
Above Dword is repeated a total of 16 times for short version

+	D11.5(ABh)+		D11.5(ABh)+			D11.5(ABh)+		D11.5(ABh)+			+
	1101	0010	1011	0100	1010	1101	0010	1011	0100	1010	
	D	2	B	4	A	D	2	B	4	A	

Above Dword is repeated a total of 255 times for long version
Above Dword is repeated a total of 15 times for short version

+	D11.5(ABh)+		D11.7(EBh)+			D20.2.(54h)-		D20.2(54h)-			-
	1101	0010	1011	0100	1000	0010	1101	0100	1011	0101	
	D	2	B	4	8	2	D	4	B	5	

-	D20.2(54h)-		D20.2(54h)-			D20.2(54h)-		D20.2(54h)-			-
	0010	1101	0100	1011	0101	0010	1101	0100	1011	0101	
	2	D	4	B	5	2	D	4	B	5	

Above Dword is repeated a total of 255 times for long version
Above Dword is repeated a total of 15 times for short version

-	D20.2(54h)-		D20.7(F4h)-			D11.5(ABh)+		D11.5(ABh)+			+
	0010	1101	0100	1011	0111	1101	0010	1011	0100	1010	
	2	D	4	B	7	D	2	B	4	A	

+	D21.5(B5h)+		D21.5(B5h)+			D21.5(B5h)+		D21.5(B5h)+			+
	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	
	A	A	A	A	A	A	A	A	A	A	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D24.3(78h)+		D24.3(78h)+			D24.3(78h)+		D24.3(78h)+			+
	0011	0011	0011	0011	0011	0011	0011	0011	0011	0011	
	3	3	3	3	3	3	3	3	3	3	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D10.2(4Ah)+		D10.2(4Ah)+			D10.2(4Ah)+		D10.2(4Ah)+			+
	0101	0101	0101	0101	0101	0101	0101	0101	0101	0101	
	5	5	5	5	5	5	5	5	5	5	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

+	D25.6(D9h)+		D6.1(26h)+			D25.6(D9h)+		D6.1(26h)+			+
	1001	1001	1001	1001	1001	1001	1001	1001	1001	1001	
	9	9	9	9	9	9	9	9	9	9	

Above Dword is repeated a total of 64 times for long version
Above Dword is repeated a total of 4 times for short version

Figure 38: Composite-Bit Pattern (COMP) starting with RD+

Long version total: 2048 Dwords total
256DW SSOP
256DW HTDP (64DW, 64DW, 64DW, 64DW)
512DW LTDP (1DW, 1DW, 509DW, 1DW)
256DW LBP
512DW LFSCP (255DW, 1DW, 255DW, 1DW)
256DW HTDP (64DW, 64DW, 64DW, 64DW)

Short version total: 128 Dwords total
16DW SSOP
16DW HTDP (4DW, 4DW, 4DW, 4DW)
32DW LTDP (1DW, 1DW, 29DW, 1DW)
16DW LBP
32DW LFSCP (15DW, 1DW, 15DW, 1DW)
16DW HTDP (4DW, 4DW, 4DW, 4DW)

Note that only 128 Dwords total for the composite pattern is too short to get a sufficient number of continuous repeats for each pattern type.

6.2.5 Hot Plug Specifications (Gen1x / Gen2x / Gen1m / Gen2m)

6.2.5.1 Hot Plug Overview

The purpose of this section is to provide the minimum set of normative requirements necessary for a Serial ATA Host or Device to be declared as "Hot-Plug Capable". As there exists various Hot-Plug events, there are relevant electrical and operational limitations for each of those types of events. The events are defined below, and the Hot-Plug Capability is further classified into:

a) Surprise Hot-Plug capable
b) OS-Aware Hot-Plug capable

When a Host or Device is declared Hot-Plug Capable without any qualifier, this shall imply that the SATA interface is Surprise Hot-Plug Capable.

For the purposes of this specification, Hot-Plug operations are defined as insertion or removal operations, between SATA Hosts and Devices, when either side of the interface is powered.

Gen1x / Gen 2x / Gen1m and Gen2m interfaces shall meet the requirements to be classified as Hot-Plug Capable. These requirements are not applicable to Gen1i and Gen2i cabled interfaces, however, Gen1i/Gen2i Devices used in Short Backplane applications shall be Hot-Plug Capable.

Hot-Plug Capable Hosts/Devices shall not suffer any electrical damage, or permanent electrical degradation, and shall resume compliant Tx/Rx operations after the applicable OOB operations, following the Hot-Plug Events.

- **Asynchronous Signal Hot Plug / Removal:** A signal cable is plugged / unplugged at any time. Power to the Host/Device remains on since it is sourced through an alternate mechanism which is not associated with the signal cable. This applies to External Single-Lane and Multi-Lane Cabled applications.
- **Unpowered OS-Aware Hot Plug / Removal:** This is defined as the insertion / removal of a Device into / from a backplane connector (combined signal and power) that has power shutdown. Prior to removal, the Host is placed into a quiescent state (not defined here) and power is removed from the backplane connector to the Device. After insertion, the backplane is powered, both the Device and Host initialize and then operate normally. The mechanism for powering the backplane on/off and transitioning the Host into/out of the "quiescent" state is not defined here. During OS-Aware events, the Host is powered. This applies to "Short" and "Long" Backplane applications.
- **Powered OS-Aware Hot Plug / Removal:** This is defined as the removal of a Device into / from a backplane connector (combined signal and power) that has power on. After insertion, both the Device and Host initialize and then operate normally. Prior to insertion or removal, the Host is placed into a quiescent state (not defined here) but the backplane connector to the Device is powered at all times. The mechanism for transitioning the Host into/out of the "quiescent" state is not defined here. During OS-Aware events, the Host is powered. This applies to "Short" and "Long" Backplane applications.
- **Surprise Hot-Plug / Removal:** This is defined as the insertion / removal of a Host or Device into / from a backplane connector (combined signal and power) that has power on. After insertion, both the Device and Host initialize and then operate normally. The powered Host or Device is not in a quiescent state.

NOTE: This does not imply transparent resumption of system-level operation since data may be lost, the device may have to be re-discovered and initialized, etc. Regardless of the above definitions, the

removal of a device which is still rotating is not recommended and should be prevented by the system designer.

6.2.5.2 Hot Plug Electrical requirements

In order to claim “Hot-Plug Capability”, Host and Devices shall implement features described in several Serial ATA specifications, not just this specification. A summary is listed here.

Serial ATA II Extensions: Cable and Connector Specification, Volumes 1 and 2:

- Defines a Backplane Connector [Volume 1]
- Defines External Single-Lane Cables/Connectors [Volume 2]
- Defines External Multi-Lane Cables/Connectors [Volume 2]
- Provides staggered pins to implement a multi-stage connection
- Provides pre-charge pins and circuits on power pins
- Provides blind-mate features
- Provides electrical shielding/grounding of cables/connectors
- Accommodates real-world connection velocities

Serial ATA Specification, Revision 1.0a

- Provides pre-charge pins and circuits on 3.3, 5.0 and 12 Volt pins
- Defines Asynchronous Signal Recovery

Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.1

- The Host PHY State Machine is modified to accommodate Asynchronous Signal Recovery (1.1)
- The Device PHY State Machine is modified to accommodate Asynchronous Signal Recovery (1.1)

This specification contains other Hot-Plug relevant electrical specifications:

- Requires AC Coupling on the Transmitter and Receiver
- Specifies a maximum AC Coupling capacitance
- Specifies the Sequencing Transient Voltage
- Specifies the Common Mode Transient Settle Time
- Provides semiconductor ESD guidelines (informative)
- Specifies grounding techniques in Disk Drive Canisters and Enclosures

6.2.5.3 Common-Mode Transients [Informative]

It is a requirement that the Hot-Plug Capable SATA component is designed to handle hot-plug events; this informative section highlights the maximum transient events encountered during hot-plug operations. An example is presented depicting some of the Hot-Plug relevant specifications of Table 2 (Sequencing Transient Voltage and Common Mode Transient Settle Time), where the impact on Hosts/Devices is shown.

The maximum current induced by a common mode transient is limited by Vcm and the minimum single-ended impedance of 42.5 ohms. Hence the worst possible surge current would be 2 volts / 42.5 ohms = 47 mA. The duration of this current is limited by the time constant, C * Rtx ~ 0.5 microseconds. This current can be further reduced by supplying common mode termination at the victim end, assuming ESD diodes do not turn on.

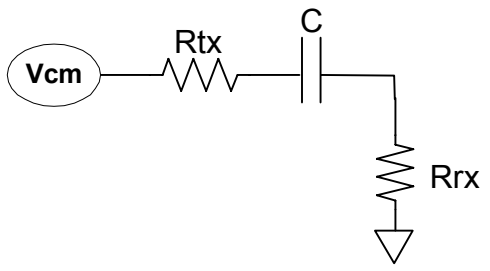


Figure 39: Example Circuit for Common Mode Transients

0 < Vcm < 2 Volts
21.25 < Rtx < 40 ohms
21.25 < Rrx < 40 ohms
C < 0.024 uF (Two 0.012 uF capacitors in parallel)

The maximum voltage step which can be transmitted to the "victim" end by a transient at the "aggressor" end is the maximum Vcm. This voltage is added to the existing bias voltage at the victim end. Since terminators have no maximum single-ended limit, this step cannot be guaranteed to be reduced by any resistive divider. Voltage transients at the "victim" end, however, may be limited by clamping action of ESD diode structures.

6.2.5.4 ESD [Informative]

There is no ESD requirement on the SATA connector interface pins. However, it is recommended that the semiconductors used in the Hot Plug Capable Hosts and Devices meet the following ESD specifications.

Receiver and Transmitter semiconductor signal pins and power pins should tolerate a minimum of 2000 V using test methods per JEDEC EIA-JESD22-A114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

Receiver and Transmitter semiconductor signal pins should tolerate 500 volts per JESD22-C101-A, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

6.2.5.5 Drive Body Discharge [Informative]

For all Serial ATA backplane systems, the Drive Canister or Enclosure should provide sufficient electrical bonding such that electrostatic potential is discharged from the drive body ground to the enclosure ground prior to the connector mating. It is strongly advised for all Serial ATA backplane systems, and Drive Canisters for hot-plug capable Devices, that the guide-rails are designed to be electrically conductive. The Drive Canister should be designed to have an electrical ground connection to device ground, and the guide-rails within the canister system should be connected to system ground.

6.2.6 Mated Pair Definition

The compliance point for receiver and transmitter is at the Device/Host I/O including the mated connector pair.

Figure 40 shows the mated connector pair detail. The compliance point includes the "tails" of the receptacle pins. The physical description of the receptacle pin tails is shown in Figure 41.

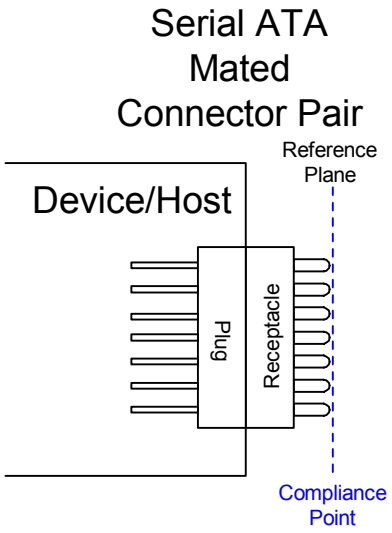


Figure 40: Mated Connector Pair

The signal interface to the mated pair connector pin tails should be done with care to minimize parasitic capacitance or inductance. The connector pin tails are a coplanar waveguide transmission line in a ground, signal, signal, ground (GSSG) configuration. The signal interface to the pin tails should maintain the GSSG configuration.

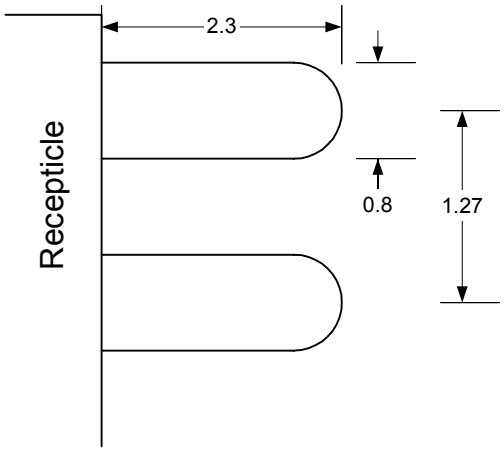


Figure 41: Mated Connector Pair, Pin Tail Detail

6.2.7 Compliance Interconnect Channels (Gen1x, Gen2x)

Compliance Interconnect Channels are defined as a set of calibrated physical test circuits applied to the Transmitter mated connector, intended to be representative of the highest-loss interconnects.

The Compliance Interconnect Channel (CIC) is used to verify that the signal electrical characteristics at the Transmitter mated connector are sufficient to ensure compliance to the input electrical specifications for Gen1x, and Gen2x receivers as delivered through worst-case media. The magnitude of this worst-case loss as a function of frequency is defined mathematically as a Transmitter Compliance Transfer Function (TCTF). There is a Gen2x TCTF and a Gen1x TCTF. Any linear, passive, differential two-port (e.g., a SATA cable) with loss greater than the TCTF at all frequencies and which meets the ISI loss constraint (defined below) is defined to be a CIC. (See also Calibration of Compliance Interconnect Channels.)

A combination of a zero-length test load (i.e., the Laboratory Load) plus the applicable CIC (Gen1x/Gen2x) is used for the specification of the host-controller or device transmitter characteristics.

A Gen1x/Gen2x transmitter signal is specified by:

1. Meeting Table 4: Transmitted Signal Requirements[1] (input swing and jitter) for Gen1x or Gen2x when transmitting into a Laboratory Load. (see sections 6.4.4, and 6.4.8)
2. Meeting Table 4: Transmitted Signal Requirements for Gen1x or Gen2x when transmitting through the appropriate Gen1x or Gen2x CIC into a Laboratory Load while using the same transmitter settings (emphasis, amplitude, etc.) as in the first test.[2]

[1] Note that the Transmitter Compliance Specifications are defined and measured into a Laboratory Load. Received signal attenuation or amplification due to actual receiver terminator tolerance as well as additional received signal ISI due to the actual receiver return loss may further degrade the actual receiver's input signal. Transmitter Compliance Specifications are expected to be only slightly tighter than Receiver Specifications.

[2] While not permitted in this specification, this second requirement can be approximated by *mathematically* processing through a TCTF the signal captured by the HBWS using only the Laboratory Load in the first requirement.

The transmission magnitude response, $|S_{21}|$, of the Gen2x TCTF satisfies the following three inequalities[3]:

$| S_{21} | \leq -20 \log_{10} (e) \{[1.7 \times 10^{-5} (f^{0.5})] + [1.0 \times 10^{-10} (f)] \}$ dB
for 50 MHz < f < 3.0 GHz, (f expressed in Hz),

$| S_{21} | \leq -10.69$dB
for 3.0 GHz < f < 5.0 GHz, and

$| S_{21} |$ at 300 MHz - $| S_{21} |$ at 1500 MHz > 3.9 dB

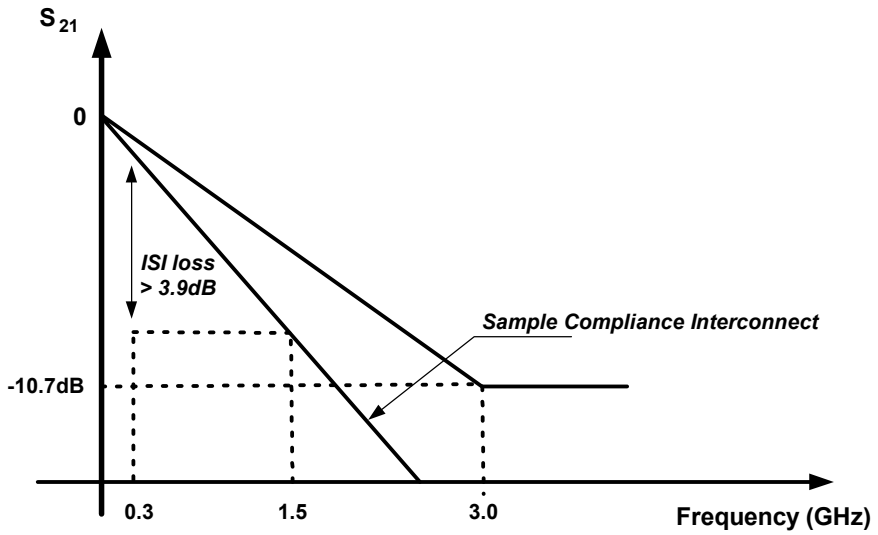


Figure 42: Compliance Channel Loss for Gen2x

The third constraint, termed ISI loss, can be motivated as follows: $|S_{21}|$ at one tenth the data rate is the attenuation of the fundamental component of a repeating five-ones-five-zeroes pattern, the longest possible run lengths in 8b/10b encoded data. Similarly, $|S_{21}|$ at one half the data rate is the attenuation of the fundamental component of a repeating …010101… pattern, the shortest possible run lengths in 8b/10b encoded data. Hence, for an output waveform of this TCTF, 2 dB approximates the ratio between a) the peak-peak voltage (established by the long run lengths) and b) the inside vertical eye opening (established by the high frequency pattern). Any TCTF with a flatter loss characteristic (i.e., with more broadband attenuation) would generate less inter-symbol interference (ISI) and therefore less output jitter. This constraint prohibits such a TCTF.

[3] Please note that "e" in the first expression is the base of the natural logarithms, approximately 2.71828. Hence, the first factor, 20 $\log_{10}(e)$, evaluates to approximately 8.6859. This value is the conversion factor from nepers (defined as the natural logarithm of a power ratio) to decibels.

The transmission magnitude response, $|S_{21}|$, of the Gen1x TCTF satisfies the following three inequalities:

$$| S_{21} | \leq -20 \log_{10} (e) \{[1.7 \times 10^{-5} (f^{0.5})] + [1.0 \times 10^{-10} (f)] \} \text{ dB}$$
for 50 MHz < f < 1.5 GHz, (f expressed in Hz),

$$| S_{21} | \leq -7.0\text{dB}$$
for 1.5 GHz < f < 5.0 GHz, and

$$| S_{21} | \text{ at 150 MHz} - | S_{21} | \text{ at 750 MHz} > 2 \text{ dB}$$

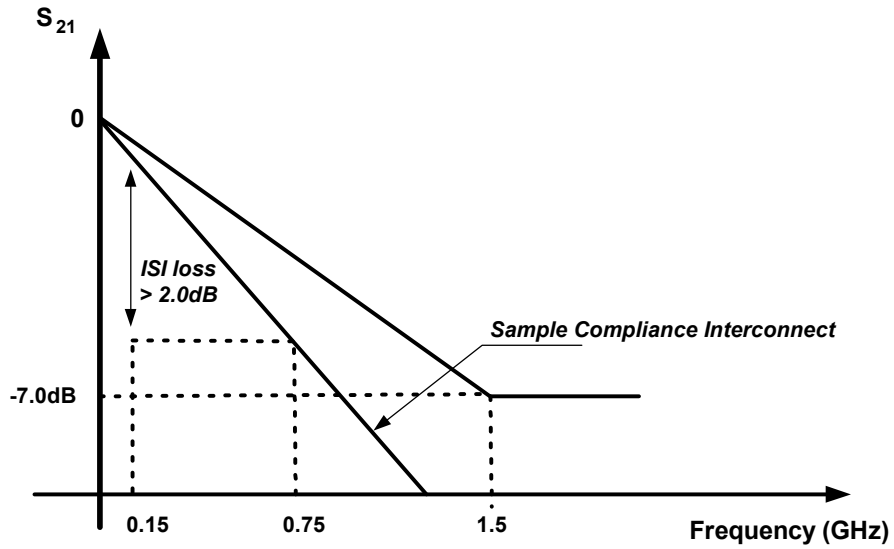


Figure 43: Compliance Channel Loss for Gen1x

6.2.7.1.1 Calibration of Compliance Interconnect Channels

The TCTF defines the worst-case loss exclusive of the two SATA connectors in the path from transmitter to receiver. However, the loss due to these two connectors shall be included in the transmitter characterization. That is, the transmitter shall be tested with the TCTF-defined loss plus two mated SATA connector pairs.

For a CIC implemented with SMA connectors, it is seen in Figure 53: Transmit Amplitude Test with Compliance Interconnect Channel that the addition of a SATA adapter (plug) following the CIC and driving into a Laboratory Load provides the required total loss of TCTF (embodied in the CIC loss) plus the loss of two SATA connectors.

6.2.8 Impedance Calibration (Optional)

The Host may employ on-chip adaptive impedance matching circuits to ensure best possible termination for both its transmitter and receiver. Device peripherals also shall provide impedance terminations, as per the specified parameters in sections Table 3: Transmitter Specifications, and Table 5: Receiver Specifications.

The Host, since it is given the first opportunity to calibrate during the power on sequence, cannot assume that the far end of the cable is calibrated yet. For this reason, the host controller must utilize a separate reference to perform calibration. In a desktop system, the cable provides the optimal impedance reference for calibration.

Using Time Domain Reflectometry (TDR) techniques, the host may launch a step waveform from its transmitter, so as to get a measure of the impedance of the transmitter, with respect to the cable, and adjust its impedance settings as necessary.

In a mobile system environment, where the cable is small or non-existent, the host controller must make use of a separate reference (such as an accurate off-chip resistor) for the calibration phase.

The device, on the other hand, can assume that the termination on the far side (host side) of the cable is fully calibrated, and may make use of this as the reference. Using the host termination as the calibration reference allows the devices operating in both the desktop and the mobile system environment to use the same hardware.

Signals generated for the impedance calibration process shall not duplicate the OOB signals, COMWAKE, COMINIT, or COMRESET. Signals generated for the impedance calibration process shall not exceed the normal operating voltage levels, cited in section 6.2. See the power management section for suggested times to perform calibration during power-on.

6.3 Jitter

This section defines jitter for SATA II, including Gen2i, Gen2x, and Gen1x. Gen 1i and measurement techniques are explained in SATA 1.0a but are copied here for completeness.

Jitter is the short-term variations of the zero crossings from ideal positions in time. A "Reference Clock" (defined in Section 6.3.2) defines the ideal positions in time. The Reference Clock method provides for the separation of jitter from SSC, tracking SSC and other low frequency modulation but not jitter. There are several types of jitter separated into two classes: deterministic and random. Deterministic jitter is bounded and random jitter is not. The amount of tolerable jitter is limited by the desired bit error rate performance of the channel. Two classes of jitter are used in analysis because they accumulate differently.

The Serial ATA data stream employs an embedded clock; no clock signal is separately sent. At the receiver, the Serial ATA data stream must be re-clocked to form a parallel digital signal. There must be enough timing margin for this process to function properly. Jitter analysis is the timing analysis used in systems with an embedded clock.

In SATA systems, random jitter is a significant portion of the total jitter so occasional errors occur. When a bit error occurs, the error is detected when an entire frame of bits is received. The bit error is corrected by retransmitting the frame; if two bit errors occur within a single frame, the corrective action is the same. The data throughput on the channel is diminished when frames are retransmitted. The goal is to maximize the data throughput and so frame error rate is the channel performance measure because it is directly related to data throughput.

Since a portion of the jitter is random, a measurement of jitter also has a random nature. That is, repeated measurements yield results that are somewhat different. As the sample size of each measurement increases, the spread of the measurement results decreases. A measured value of random jitter is known to a confidence level.

A frame error rate test is a system performance test done on a combination of SATA compliant components. To achieve a statistically significant estimate of the frame error rate a large sample size is necessary. A frame error rate test on a SATA channel is lengthy requiring about an hour at Gen2 rates.

Jitter tests are compliance tests done on an individual SATA component, a device, host, or interconnect to ensure system performance. Compliance tests predict performance of combinations of compliant components. It is often highly desirable to make jitter measurements in a short period of time rather than hours. Consequently, jitter measurements are done with small sample sizes and the results are extrapolated to predict results with larger sample size.

Extrapolation of results from small sample size to large sample size involves assumptions. This specification defines two assumptions to use and takes these as normative or a required portion of the specification. First, the random jitter has a Gaussian distribution. Second, the total jitter is the sum of the deterministic jitter and 14 times the standard deviation of the random jitter. These allow the separation of deterministic from random jitter, and an estimate of the total jitter for an equivalent BER of 10^{-12} from a much smaller sample size.

6.3.1 Definition

For Gen1x, Gen2i and Gen2x, jitter is defined as the difference in time between a data transition and the associated Reference Clock event. The jitter at the receiver is the result of the aggregate jitter in the transmission path. First, jitter is generated during clocking of the data in the transmitter. Then, each element in the channel between the transmitter and the receiver influences the jitter. Finally, the receiver shall be able to recover the data despite the jitter, otherwise errors occur. The receiver jitter tolerance shall be greater than the transmitter's generated jitter and the expected jitter accumulation through the channel.

Jitter budgets are dependent on the desired bit error rate (BER). SATA assumes a BER target of less than 10^{-12}. For Gen1x, Gen2i and Gen2x, SATA II jitter levels are defined as Reference Clock to data. The Reference Clock is extracted from a serial data stream using either a PLL (hardware) or a clock recovery algorithm (software). For Gen1i, SATA 1.0a, which defines jitter as data to data, remains unchanged.

The Reference Clock to data jitter methodology allows for jitter measurements to be made on a device or host using a Spread Spectrum Clock or a non-spreading clock.

6.3.2 Reference Clock Definition

The Reference Clock is defined as that clock recovered from a Serial ATA data stream. The Reference Clock provides the distinction between Spread Spectrum Clocking (SSC) and jitter. The Reference Clock tracks SSC and wander, but not jitter. In addition, it provides a definition for determining the SSC profile.

Reference Clock extraction is performed using either hardware or software PLLs. Two Reference Clock PLLs are defined as type 2 PLL with a -3dB corner frequency $f_{c3dB} = f_{BAUD}/N$ (N = 10 (Gen2i), 500 (Gen2i), 1667 (Gen1x, Gen2x)) given a transition density of 1.0 (corresponding to a 1010101010 clock-like pattern) and damping factor ξ = 0.707 min to 1.00 max. This frequency dependent shape assumes that the Clock and Data Recovery circuit (CDR) can track low frequency modulation and SSC. Since SATA receivers need to recover the signal from a spread spectrum transmitter or a non-spreading transmitter, this clock extraction eliminates the spread spectrum frequency modulation from the jitter measurements.

At least two receiver architectures are possible within the SATA specification – over-sampling and tracking. Over-sampling architectures can respond to data period changes quickly while tracking architectures tend to have a slower response time.

Several corner frequencies are provided in the jitter budget ($f_{c3dB} = f_{BAUD}/10$ (Gen2i), $f_{c3dB} = f_{BAUD}/500$ (Gen2i), and $f_{c3dB} = f_{BAUD}/1667$ (Gen1x, Gen2x)). Transmitters and receivers shall meet both specifications.

6.3.3 Spread Spectrum Clocking

Serial ATA allows the use of spread spectrum clocking, or intentional low frequency modulation of the transmitter clock. The purpose of this modulation is to spread the spectral energy to mitigate the unintentional interference to radio services. The modulation frequency of SSC shall be in the range defined for f_{SSC} in Table 2.

The modulation frequency deviation shall be in the prescribed range for SSC_{tol} in Table 2. The instantaneous frequency (each period) of the Reference Clock shall fall within the prescribed T_{UI} range. If the rate of change of the instantaneous frequency is excessive jitter is increased.

The SSC modulation only moves the frequency below the nominal frequency. This technique is often called "down-spreading". An example triangular frequency modulation profile is shown in Figure 44. The modulation profile in a modulation period can be expressed as:

$$f = \begin{cases} (1-\delta) f_{nom} + 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad 0 < t < \dfrac{1}{2 f_m}; \\ (1+\delta) f_{nom} - 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad \dfrac{1}{2 f_m} < t < \dfrac{1}{f_m}, \end{cases}$$

where f_{nom} is the nominal frequency in the non-SSC mode, f_m is the modulation frequency, δ is the modulation amount, and t is time.

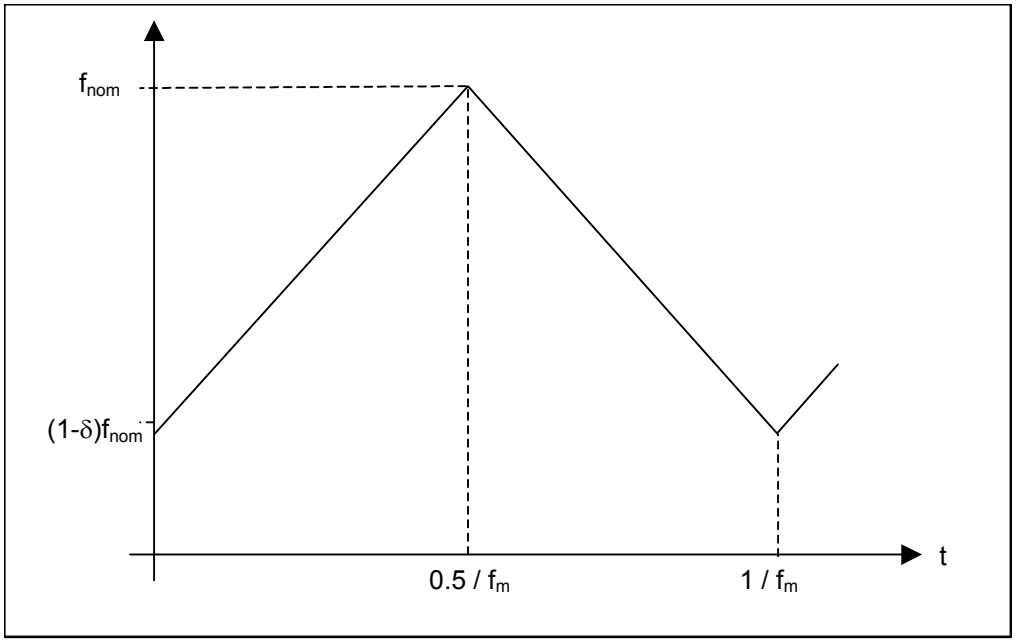


Figure 44: SSC Profile Example: Triangular

As an example, for triangular modulation, the absolute spread amount at the fundamental frequency is shown in Figure 45, as the width of its spectral distribution.

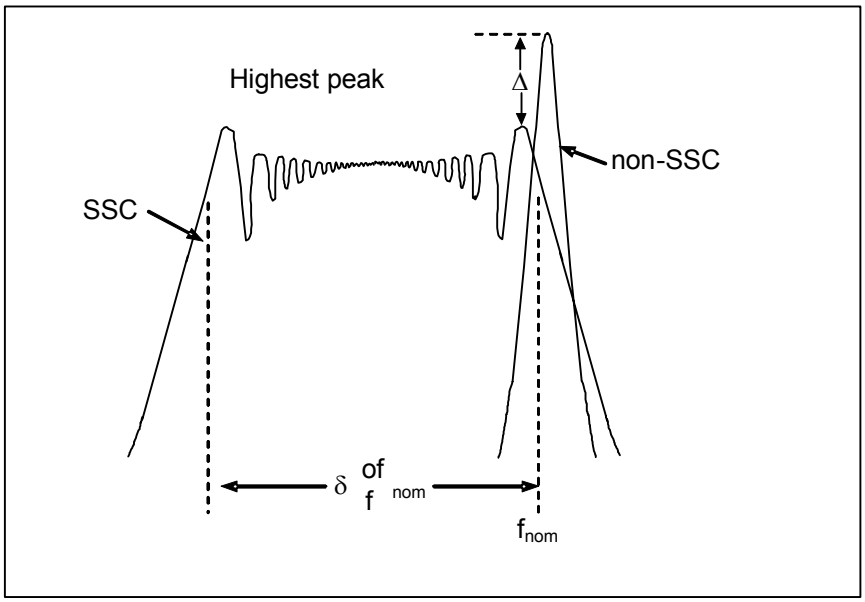


Figure 45: Spectral fundamental frequency comparison

6.3.4 Jitter Budget

There are two types of jitter, random jitter (RJ) and deterministic jitter (DJ). Random jitter is Gaussian and unbounded. For ease, the standard deviation (RJ_σ) is multiplied by a factor which corresponds to the required BER. For a BER = 10^{-12}, the associated multiplication factor for Serial ATA is 14.

Total jitter (TJ) for SATA II is peak-to-peak and defined as:

$$TJ = (14 * RJ_\sigma) + DJ$$

Table 4: Transmitted Signal Requirements and Table 6: Lab-Sourced Signal (for Receiver Tolerance Testing) show the compliance jitter values. The measurement of jitter is described in section 6.4.7.

6.3.5 Jitter Formulas without SSC-[Informative]

6.3.5.1 Clock to Data

Consider the times when the clock edges occur. A perfect clock has edges that occur at multiples of a given period T. Associate an integer index with each clock edge. The times of ideal clock edges is expressed by

$$t_C(i) = i\,T$$

Data transitions always occur on a clock edge. Ideal data transitions occur at the same times as clock edges. In real systems, the data transitions do not occur at ideal times. The time error from ideal of the data transitions is called the "clock to edge jitter". This is expressed by

$$t_D(i) = i\,T + \varepsilon_i$$

where the ε_i are time deviations from ideal, the clock to edge jitter. Over time, these perturbations are constrained by

$$\lim_{N\to\infty} \sum_{i=0}^{N-1} \frac{\varepsilon_i}{N} = 0$$

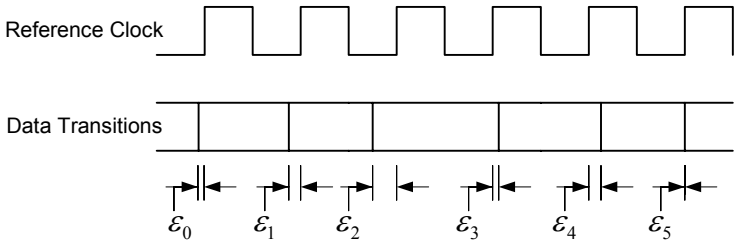


Figure 46: Jitter Deviations

6.3.5.2 Data to Data

The time difference between data transitions is shown in Figure 47: Edge to Edge Timing and given by

$$t_D(j) - t_D(i) = \left(j - i\right)T + \varepsilon_j - \varepsilon_i$$

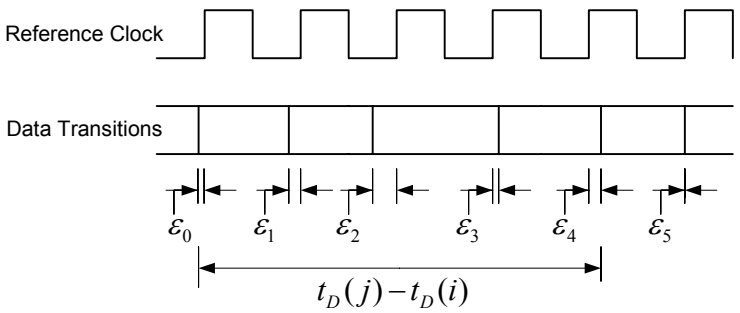


Figure 47: Edge to Edge Timing

A specification must be invariant to when the measurement is taken so introduce a new quantity $k = (j - i)$ for the spacing between bits. The time difference between data transitions is

$$t_D(i+k) - t_D(i) = k\,T + \varepsilon_j - \varepsilon_i$$

Define a new quantity for the limits of this time difference--this is jitter as defined in the SATA 1.0a specification. Note the maximum and minimum is taken over all bit positions i, which makes the jitter a function of only the bit spacing k.

$$t_J(k) = \max\left[t_D(i+k) - t_D(i)\right]_{\forall i} - \min\left[t_D(i+k) - t_D(i)\right]_{\forall i}$$

$$t_J(k) = \max\left[k\,T + \varepsilon_{i+k} - \varepsilon_i\right]_{\forall i} - \min\left[k\,T + \varepsilon_{i+k} - \varepsilon_i\right]_{\forall i}$$

Note that kT is a constant for each k, and is present in both the maximum and minimum terms. Since the difference is taken, the terms cancel giving

$$t_J(k) = \max\left[\varepsilon_{i+k} - \varepsilon_i\right]_{\forall i} - \min\left[\varepsilon_{i+k} - \varepsilon_i\right]_{\forall i}$$

A distinct advantage of this jitter definition is the absence of dependence on the bit time T. This is not true when the clock is frequency modulated as in spread spectrum clocking (SSC).

For a given separation of data transitions expressed in clock cycles, the maximum peak to peak deviation of the data transition spacing is the jitter defined in SATA 1.0a. It is a function of the transition separation only, not the position of any particular transition. This jitter definition expresses the extreme separations of data transition times.

6.4 Measurements

The performance of a SATA system with host and device connected together is measured by the frame error rate, using a set of reference frames, defined by a specific set of ordered test patterns within the frame. A Host or Device is commanded to generate the various test patterns through the use of the BIST FIS Serial ATA command or other vendor unique commands to the device under test.

Measurements of devices and hosts are done to determine compliance with this specification. Compliance tests are done with a device or host connected to test equipment. Compliance tests are not done with devices and hosts connected together. Unless otherwise specified, all compliance measurements shall be taken through the mated connector pair.

The values specified in Table 4: Transmitted Signal Requirements refers to the output signal from the unit under test at the mated connector into a Laboratory Load. The signals are not specified when attached to a system cable or backplane.

The values specified in Table 6: Lab-Sourced Signal (for Receiver Tolerance Testing) refers to the input signal from any signal source as measured at the unit under test using a Laboratory Load.

The components that make up the system each affect the system's performance, not simply by summing up the low-level parameters. There are many interactions as well as protocol effects such as the retry algorithms.

Fundamental to specification is a clear definition of the UUT (unit under test). The UUT consists of the host/device and the receptacle side of the mated pair connector. This places the signals at a point in the test measurement setup where all specifications of the UUT are defined at an impedance level of 50 ohms each signal line to ground which is 100 ohms differential and 25 ohms common mode impedance. This is the compliance point for hosts and devices.

The Serial ATA physical layer compliance shall be tested using the Parametric Method. This method uses repetitive patterns and a Laboratory Load to allow accurate, repeatable measurements to be performed on the unit under test.

Additional measurement methods for several parameters are aimed at providing quick No-Go testing. These use any valid data pattern and a Laboratory Load to quickly produce a visual "picture" of the performance of the unit under test. For example, one measurement method uses Data Eyes to quickly understand jitter. Another uses a mode measurement for identifying a potentially complex signal with a single amplitude value. However, none of these No-Go measurement methods may be used for testing compliance to electrical specifications. These measurement methods are valuable for gaining useful information about the performance of the unit under test which goes beyond specification compliance issues.

Both methods produce measurements of electrical performance, however, the parametric method shall be used for validation of the unit under test to the Serial ATA requirements 6.2 while other methods may be used as general No-Go tests.

6.4.1 Frame error rate testing

Frame error rate is the measure of link performance, a system level test. Since bit errors are ignored except during frames, frame error rate testing is used as the method of measuring channel performance during system operation.

Serial ATA error detection at the frame level uses the CRC (Cyclic Redundancy Check) error detection mechanism, and respective reporting to the higher layer levels. Since all frames include a header and CRC field, the calculation includes these overhead bytes in the Frame Error specification.

The bit error rate is a measurement of raw channel performance and is closely related to the PHY parameters. The measurement of bit error rate is complicated by the 8b/10b encoding and SATA protocol. A single bit error may result in several related errors occurring closely together which in turn may result in multiple bit-error counts. A character might have a single bit error in it that causes a code-violation error. A disparity error might occur on a following character, caused by the same single error. A single bit error has a high probability of causing a byte-wise error, or an 8b/10b code violation error, due to the 8b/10b encoding, thus a single bit error translates to 8-bits or 10-bits of error. A missing or an extra bit detected by the receiver will, translate into a series of errors that spans across multiple byte-boundaries until bit re-alignment via ALIGN primitives.

6.4.1.1 Frame error-rate patterns

Frame error rate patterns contain the elements of the bit error rate test bit patterns and sequence of patterns, so as to thoroughly stress the serial interface in the system, while using the higher level CRC error detection and reporting from the lower protocol level layers to the Application level layer.

The frame patterns shall be comprised of the set of the Composite Patterns, cited in section 6.2.4.3.6, but with the parameters extended so as to achieve the maximum frame length.

Note that the compliant patterns shown are the patterns that are expected on the wire. When sent using a normal FIS payload mechanism the data within a FIS is scrambled. For the correct patterns to appear on the wire “pre-scrambling” must be performed so that the specified patterns appear after any payload scrambling performed by the transport layer.

6.4.1.2 Frame error-rate measurements

The Frame Error Rate (FER) shall be measured and computed to be no greater than $8.200*10^{-8}$ at a 95% confidence level when tested with any given 8b/10b pattern, including the Frame-Error-Rate reference patterns cited in section 6.4.1.1. The Serial ATA CRC error detection mechanism is used to measure FER.

The frame error rate is calculated based on the maximum size of a Data FIS, plus overhead for the FIS header and CRC Dwords. The Frame Error Rate assumes a target bit error rate of 10^{-12}.

$$FER = \left(8192 + 8\right) \times 10 \times 10^{-12} = 8.200 \times 10^{-8}$$

Note that the cited patterns should appear on the wire, and the parameters of the reference patterns shall be extended to achieve the maximum frame length of 8192 user payload bytes.

6.4.1.3 Amount of data to transfer to achieve target confidence level - [Informative]

As this is a statistical process, there are confidence levels associated with each measurement that is related to the number of frames transferred. For example, one can only declare that the interface Frame-Error-Rate performance has been achieved with a confidence level for that given sample size, and Error-thresholds as shown in Table 8.

Table 8: Confidence Levels versus Sample Size

Sample Size (Frames)	Number of Frame-Errors										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
$1.22*10^7$	63.21%	26.42%	8.03%	1.90%	0.37%	0.06%	0.01%	<0.01%	<0.01%	<0.01%	<0.01%
$1.22*10^8$	>99.99%	99.95%	99.72%	98.97%	97.07%	93.29%	86.99%	77.98%	66.72%	54.21%	41.70%

The sample size is taken as ten times the total number of frames transmitted for a given error rate.

$$\frac{1}{8.2\times10^{-8}}\times10 = 1.22\times10^{8}$$

Thus, the minimum number of frames required to declare a Frame Error Rate of $8.200*10^{-8}$ with confidence level of >95% is $1.22*10^8$ frames.

6.4.1.4 Bit Error Rate Testing--[Informative]

There are two basic classes of errors that will affect the bit-error rate performance that have to be considered: bit-errors, and burst-errors.

In order to get a fair assessment of bit-error-rate performance, bit-errors, as well as burst errors, must be considered separately. This is because a missing or an extra bit detected by the receiver will translate into a series of errors that spans across multiple byte boundaries until re-alignment via an alignment sequence. This series of errors will be defined as burst errors.

Another type of byte-wise error exists when an entire byte is not received. As viewed by the higher level protocol it will appear as a loss of word synchronization. It will cause a burst error whose span can be limited by higher-layer protocol transmission conventions at the next alignment sequence.

Any of these errors may result in several related errors occurring closely together which in turn may result in multiple apparent bit-error events. For example, a character might have a single bit error in it that causes a code-violation error. A disparity error might occur on a following character, caused by the same single error.

All of these events eventually are recognized during the decoding process and will result in a frame error.

NOTE: Burst Error Rate measurements shall not be used for Compliance testing.

6.4.1.4.1 Bit error rate measurements [Informative]

The Bit error rates, if measured and computed, byte-wise, should be no greater than 10^{-12} bit-errors when tested with the reference test patterns, cited in section 6.4.1.1.

Note that the Frame-Error Rate measurements constitute the basis for the applicable test requirements for this specification.

6.4.1.4.2 Amount of data to transfer to achieve target error rate [Informative]

As this is a statistical process, there are confidence levels associated to each sample size. For example, one can only declare that the interface Bit-Error-Rate performance has been achieved with a confidence level of 95% for that given sample size, and Error-thresholds as shown in Table 9.

Table 9: Confidence Levels versus Sample Size (with Error Thresholds)

Sample Size (Bits)	Number of Bit-Error Events - Threshold										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
$1.00*10^{12}$	63.21%	26.42%	8.03%	1.90%	0.37%	0.06%	0.01%	<0.01%	<0.01%	<0.01%	<0.01%
$1.00*10^{13}$	>99.99%	99.95%	99.72%	98.97%	97.07%	93.29%	86.99%	77.98%	66.72%	54.21%	41.70%

Thus, the minimum number of Bits required to declare a Bit-Error-Rate 10^{-12} with confidence with confidence level of >95% should be (10^{13}) Bits.

6.4.2 Measurement of Differential Voltage Amplitudes

The differential voltage amplitude, V_{diffTX}, shall be measured for bits in representative data patterns. It is necessary to use patterns that are DC balanced for this testing (otherwise, an offset will be introduced that will shift the measured mean values).

The test setup shown in Figure 48 below shows the connections:

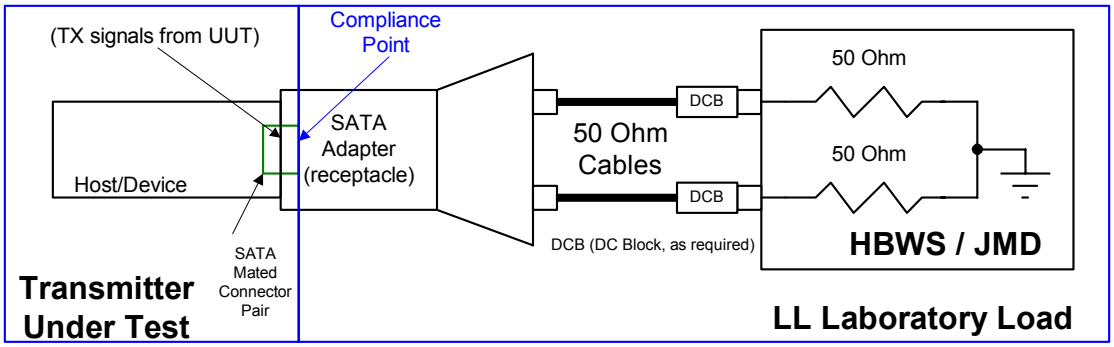


Figure 48: Differential Voltage Amplitude Measurement

The transmitter under test sends the test pattern to a HBWS. The differential voltage waveform corresponding to one complete cycle of the N bit pattern will have some unit intervals corresponding to 0 bits and some unit intervals corresponding to 1 bits. Figure 49 illustrates an example of a display on an equivalent time scope:

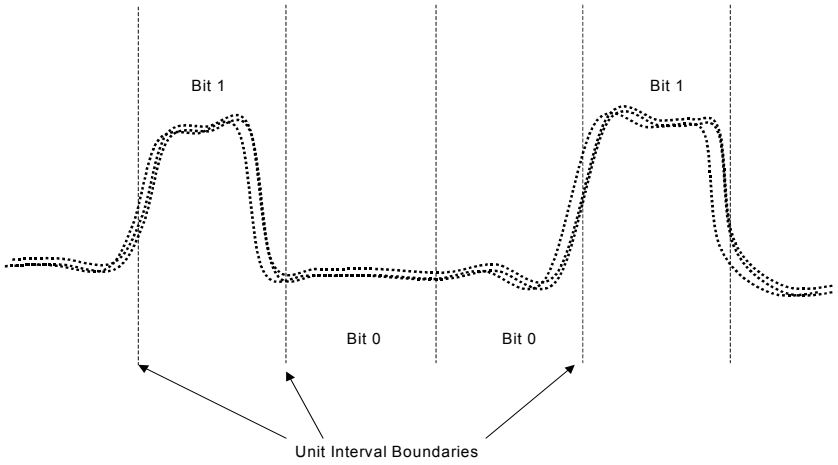


Figure 49: Differential Voltage Amplitude Measurement Pattern Example

6.4.2.1 Testing for Minimum Differential Voltage Amplitude

There are two separate procedures for this testing. However, each of the two procedures requires a common set of steps to be performed. These are labeled below as “Common Steps”. Following these steps are those which describe the rest of the procedure for one of two options (labeled as “Option 1 or Option 2 Steps”).

Common Steps:

Common Step 1: Transmitting a HFTP pattern, for a unit interval (UI) corresponding to a 1 bit, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \le n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

The inequality above is based on a requirement that enough samples are collected to define a confidence interval with at least 95% probability and with a width no greater than 10% of the sample mean.

Compute the following value:

$$UH = [\bar{x} - \frac{1.96s}{\sqrt{n}}]$$

Common Step 2: Transmitting a HFTP pattern, for a unit interval (UI) corresponding to a 0 bit, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \le n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$LH = [\bar{x} + \frac{1.96s}{\sqrt{n}}]$$

Common Step 3: Transmitting a MFTP pattern, for a unit interval (UI) corresponding to the 2nd 1 bit of a string of 2 consecutive 1 bits, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$UM = [\bar{x} - \frac{1.96s}{\sqrt{n}}]$$

Common Step 4: Transmitting a MFTP pattern, for a unit interval (UI) corresponding to the 2nd 0 bit of a string of 2 consecutive 0 bits, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$LM = [\bar{x} + \frac{1.96s}{\sqrt{n}}]$$

Common Step 5: Compute the minimum of the following two differences:

DH = UH – LH
DM = UM – LM

That is, compute DHM = min (DH, DM).

This value will be used in the final step of each of the following two options.

6.4.2.1.1 Lone Bit Pattern measurements, Option 1

If the test environment allows for the creation of a pattern trigger, the LBP pattern is used to make the following measurements. Continue the procedure from Common Step 5 above with the following steps for Option 1.

If the test environment does not allow for the creation of a pattern trigger, the continue the procedure from Common Step 5 above with the steps beginning with Option 2 Step 6 below.

Option 1 Step 6: Transmitting a LBP pattern, for a unit interval (UI) corresponding to a lone 1 bit, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$A = [\bar{x} - \frac{1.96s}{\sqrt{n}}]$$

Option 1 Step 7: Transmitting a LBP pattern, for a unit interval (UI) corresponding to a lone 0 bit, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$B = [\bar{x} + \frac{1.96s}{\sqrt{n}}]$$

Option 1 Step 8: From A and B obtained in steps 1 and 2, compute:

VTestLBP = A – B

Then take the miniumum of VTestLBP and the previously computed DHM (from Common Step 5), that is,

VTest = min (VTestLBP, DHM)

The test for minimum amplitude is passed if:

VTest > V_{diffTX}(Min)

(see Table 4: Transmitted Signal Requirements, Section 6.2.1 for V_{diffTX}(Min)). Otherwise, the test for minimum differential voltage amplitude has not been passed. If the test for minimum voltage amplitude is failed, the number of samples, n, is to be increased and the test must be executed again for this larger number of samples. Failure to arrive at a value n for which the test will pass means that the requirement of the specification for minimum differential voltage amplitude has not been met.

6.4.2.1.2 Approximation to Lone Bit Pattern measurements, Option 2

To test for minimum differential voltage amplitude without the ability to create a pattern trigger, continue the procedure from Common Step 5 above with the following steps for option 2:

Option 2 Step 6: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the first 1 bit that follows either a string of 3 preceding 0 bits or a string of 4 preceding 0 bits. It is required that the histogram samples be the union of the samples collected for both cases. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$A = [\bar{x} - \frac{1.96s}{\sqrt{n}}]$$

Option 2 Step 7: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the first 0 bit that follows either a string of 3 preceding 1 bits or a string of 4 preceding 1 bits. It is required that the histogram samples be the union of the samples collected for both cases. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Compute the following value:

$$B = [\bar{x} + \frac{1.96s}{\sqrt{n}}]$$

Option 2 Step 8: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the last 1 bit in a string of 3 or 4 1 bits. It is required that the histogram samples be the union of the samples collected for both cases. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Call the mean, $\bar{x} = C$

Option 2 Step 9: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the last 0 bit in a string of 3 or 4 0 bits. It is required that the histogram samples be the union of the samples collected for both cases. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Call the mean, $\bar{x} = D$

Option 2 Step 10: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the last 1 bit in a string of 4 1 bits. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Call the mean, $\bar{x} = \mathrm{E}$

Option 2 Step 11: Transmitting a LFTP pattern, construct a histogram based on n samples collected in the waveform epoch [0.45UI, 0.55UI] for the UI of the last 0 bit in a string of 4 0 bits. The number of samples in a histogram (n) for the UI must be greater than or equal to 100 and must meet the requirement that:

$$1537(s/\bar{x})^2 \leq n$$

where:

$\bar{x} =$ the mean of the voltage samples in the histogram which can be read from the HBWS in histogram measurement mode

s = the standard deviation of the voltage samples in the histogram which can also be read from the HBWS

n = the number of samples that contribute to the histogram – this can also be read from the HBWS

Call the mean, $\bar{x} = \mathrm{F}$

Option 2 Step 12: From A and B obtained in steps 1 and 2, compute:

VTestAPP = (A + C + F) – (B + D + E)

Then take the miniumum of VTestAPP and the previously computed DHM, that is,

VTest = min (VTestAPP, DHM)

The test for minimum amplitude is passed if:

$VTest > V_{diffTX}(Min)$

(see Table 4: Transmitted Signal Requirements, Section 6.2.1 for $V_{diffTX}(Min)$). Otherwise, the test for minimum differential voltage amplitude has not been passed. If the test for minimum voltage amplitude is failed, the number of samples, n, is to be increased and the test must be executed again for this larger number of samples. Failure to arrive at a value n for which the test will pass means that the requirement of the specification for minimum differential voltage amplitude has not been met.

The following figure illustrates the locations of the sections of the LFTP as displayed on a scope from which the measurements of the values for A,B,C,D,E, and F (see steps 1 through 6 above) are to be made.

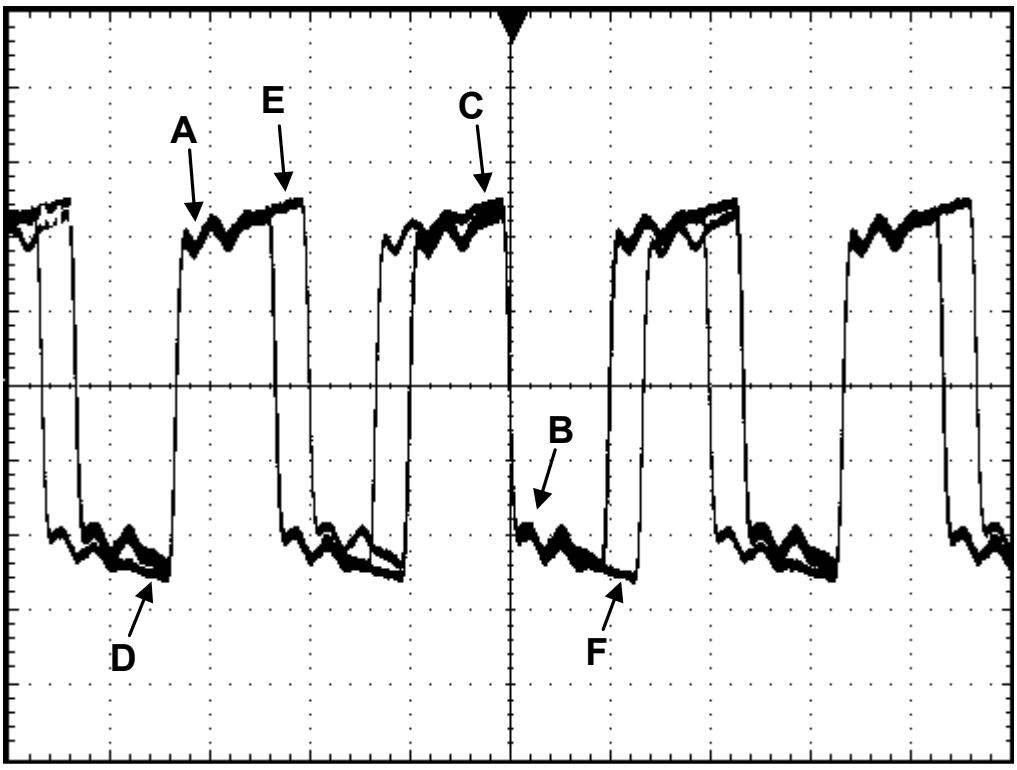


Figure 50: LFTP Pattern on High BW Scope (HBWS)

6.4.2.2 Test for Maximum Differential Voltage Amplitudes

To test for maximum differential voltage amplitude for a given data pattern, perform the following steps using the LFTP and the MFTP as the data patterns. The waveform sections to be examined are defined as:

High Test UI:

For the LFTP, use the 4th 1 bit in a string of 4 1 bits.
For the MFTP, use the 1st 1 bit in a string of 2 1 bits.

Low Test UI:

For the LFTP, use the 4th 0 bit in a string of 4 0 bits.
For the MFTP, use the 1st 0 bit in a string of 2 0 bits.

Step 1: For the High Test UI, construct a histogram in the waveform epoch [0.0UI, 1.0UI] for the UI. Position the upper edge of the histogram window at VU mV where:

$$VU = \frac{1}{2} V_{DIFFTX}(\max)$$

See Table 4: Transmitted Signal Requirements, Section 6.2.1 for V_{diffTX}(Max).

Position the lower edge of the histogram window at 0 mV. Let the histogram acquire hits for a fixed time duration, T, such that the number of hits acquired is at least 10000. Note the number of histogram hits as NU. This histogram can be based on data stored in the waveform database.

For the same High Test UI, construct a histogram in the waveform epoch [0.0UI, 1.0UI]. Position the upper edge of the histogram window at VU + 300 mV. Position the lower edge of the histogram window at VU mV. Note the number of histogram hits as nu.

Step 2: For the Low Test UI, construct a histogram in the waveform epoch [0.0UI, 1.0UI]. Position the upper edge of the histogram window at 0 mV. Position the lower edge of the histogram window at VL mV where:

$$VL = -\frac{1}{2} V_{DIFFTX}(\max)$$

Let the histogram acquire hits for the same fixed time duration, T, as used in step 1. (In practice, using the same waveform database as that collected in Step 1 insures that the same time duration is examined.) Note the number of histogram hits as NL.

For the same Low Test UI, construct a histogram in the waveform epoch [0.0UI, 1.0UI]. Position the lower edge of the histogram window at VL - 300 mV. Position the upper edge of the histogram window at VL mV. Note the number of histogram hits as nl.

Step 7: Compute the values:

$$pu = \frac{nu}{nu + NU}$$

$$pl = \frac{nl}{nl + NL}$$

(Note: there will be two values of pu and pl computed; one for the use of the LFTP and one for the use of the MFTP).

Step 8: The test for maximum amplitude is passed if:

pu < 0.05

and

pl < 0.05

(Note: Since there are two values of pl and pu, the test must be applied to each pair.)

Otherwise, the test for maximum differential voltage amplitude has not been passed.

6.4.3 Rise and Fall Times

The rise and fall times of the waveform under test are defined over a 20%-80% output level change from the High and Low reference levels. High Reference level of the waveform under test is the “mode” of the top portion while the Low Reference level is the “mode” of the bottom portion. Mode is measured using Statistical Methods of the desired waveform and is the most common value of the probability density function.

Therefore, Rise Time = X2 - X1; where X2 is the mean horizontal time value corresponding to 80% of the distance between the Low and High value and X1 is the mean horizontal time value position corresponding to 20% of the distance between the Low and High value.

And Fall Time = X1 - X2; where X1 is the mean horizontal time value corresponding to 20% of the distance between the Low and High value and X2 is the mean horizontal time value position corresponding to 80% of the distance between the Low and High value.

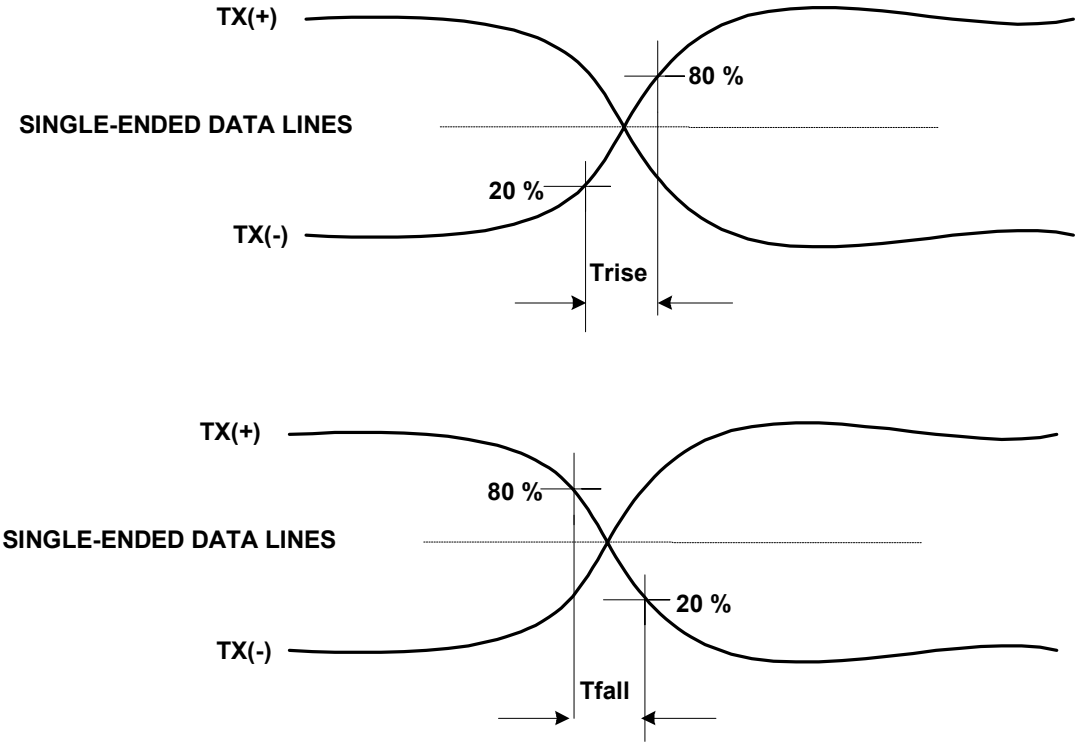


Figure 51: Single Ended Rise and Fall Time

Rise and Fall values are measured using the HFTP, LFTP, and Lone Bit Patterns previously defined.

The rise and fall times for transmitter differential buffer lines are measured with the load fixture shown in Figure 52. The rise and fall times shall be measured with an HBWS.

6.4.4 Transmitter Amplitude

The transmitter amplitude values specified in Table 4: Transmitted Signal Requirements refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1x, and Gen2x), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen1x and Gen2x only). The signals are not specified when attached to a system cable or backplane.

Transmitter amplitude is measured with each of three waveforms: HFTP, LFTP, and the Lone bit pattern. Amplitude specifications shall be met during each bit within the specified patterns. For example, the “lone-bit” within the Lone Bit Pattern is often of lower amplitude than most bits.

The minimum amplitude value is measured 0.5UI after a Reference Clock edge (defined in section 6.3.2). The Reference Clock defines the ideal (zero jitter) zero crossing times. The maximum amplitude is measured across the entire waveform.

The transmit DC offset voltage (for Gen1i only) can be measured with the setup in Figure 52. The HBWS is measuring a DC voltage and the DC blocks must not be present.

Figure 52 and Figure 53 show test setups for measuring transmitter amplitude. The HBWS is the standard for measuring amplitude. The losses in the test connections can be significant so it is prudent to minimize and estimate these. Several methods can be used to estimate the cabling losses. The first is to use two cables of different lengths and compare the losses of each. The second is to rely on published data for the cables. The third is to obtain a separate means for measuring the cable loss such as characterization with a network analyzer or power meter.

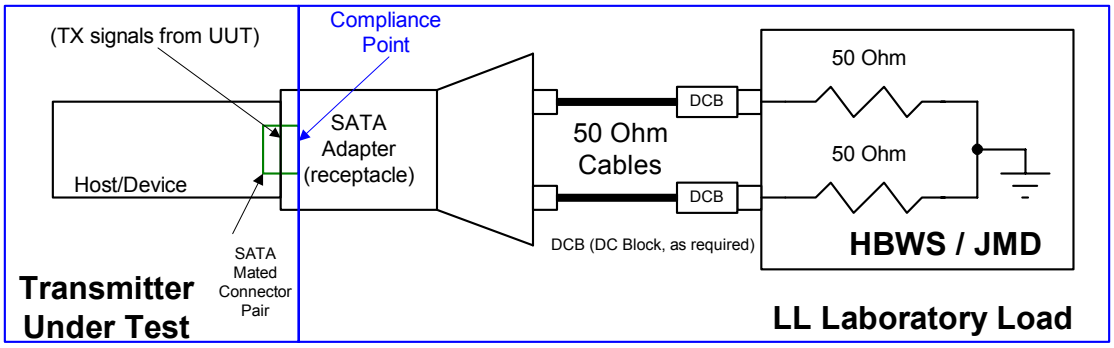


Figure 52: Transmit Amplitude Test with Laboratory Load

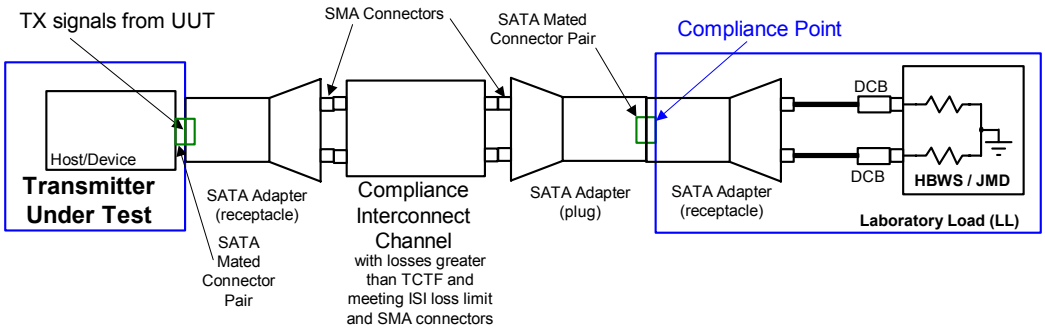


Figure 53: Transmit Amplitude Test with Compliance Interconnect Channel

This specification describes transmitter levels in terms of voltage when driving a test load of 100 ohms differential (the Laboratory Load, LL) and 50 ohms single ended to ground. To relate the specified maximum levels to the maximum values seen in a system requires a calculation. An example of this calculation is in section 6.4.5.

6.4.5 Receive Amplitude

This section describes setting the receive amplitude, a test condition common to many tests. The proper operation of the receiver is its ability to receive a signal. An example of this testing is described in 6.4.9. The values as specified in Table 6 refer to the input signal from any signal source as measured at the device under test using a Laboratory Load.

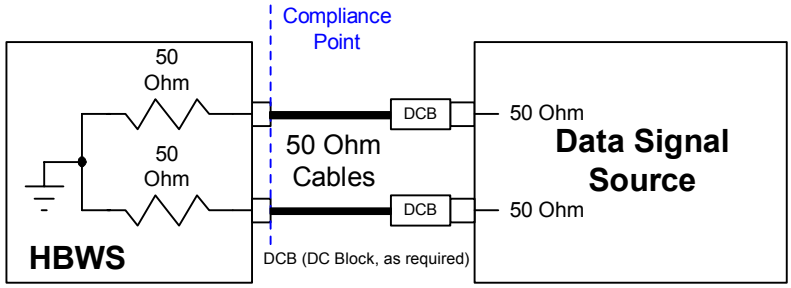


Figure 54: Receiver Amplitude Test--Setting Levels

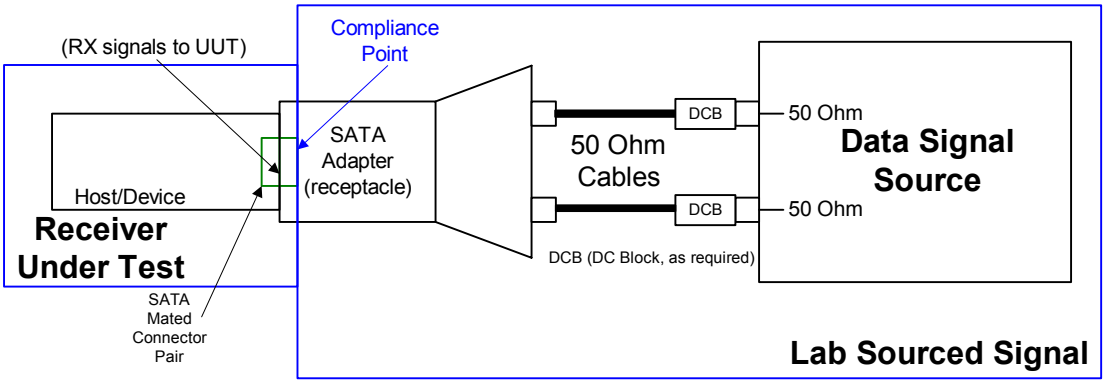
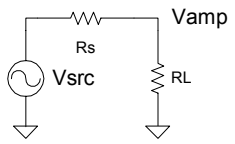


Figure 55: Receiver Amplitude Test

Figure 54: Receiver Amplitude Test--Setting Levels shows an example to account for loss in the cabling and error in the signal source for receiver level testing. The loss in the SATA adapter is not accounted for here, but can be separately measured. The HBWS is used as the standard for amplitude when setting the levels for testing receivers. Equivalent methods to account for loss in the cabling are acceptable.

This specification describes receiver levels in terms of voltage driven from a differential source of 100 ohms impedance. A calculation is required to relate the specified maximum receiver level to the maximum receiver level in a system. The maximum receiver level is set at a HBWS by driving with a signal source impedance of 100 ohms. With the signal generator level set, it is then applied to the receiver under test. The voltage actually seen at the receiver inputs depends on the input impedance of the receiver. The maximum voltage at the receiver occurs when the receiver input impedance is at its maximum value.



$$V_{AMP} = \frac{V_{SRC}}{\left(1+\frac{R_S}{R_L}\right)} = \frac{V_A\left(1+\frac{R_S}{R_{LL}}\right)}{\left(1+\frac{R_S}{R_L}\right)}$$

The values of the receiver and transmitter resistor termination is set by the return loss specification at low frequency. Return loss is given by the following equation:

$$RL = -20\log\left[\left|\frac{Z-Z_0}{Z+Z_0}\right|\right]$$

And solving this for the resistance, the real part of the impedance gives two solutions

$$R = Z_0\frac{1-10^{-RL/20}}{10^{-RL/20}+1} = (100)\frac{1-10^{-18/20}}{10^{-18/20}+1} = 77.64$$

$$R = Z_0\frac{10^{-RL/20}+1}{1-10^{-RL/20}} = (100)\frac{10^{-18/20}+1}{1-10^{-18/20}} = 128.8$$

$$R = Z_0\frac{1-10^{-RL/20}}{10^{-RL/20}+1} = (100)\frac{1-10^{-14/20}}{10^{-14/20}+1} = 66.73$$

$$R = Z_0\frac{10^{-RL/20}+1}{1-10^{-RL/20}} = (100)\frac{10^{-14/20}+1}{1-10^{-14/20}} = 149.9$$

The highest amplitude that can be seen at the receiver occurs when the receiver input resistance is highest.

$$V_{AMP} = \frac{0.7\left(1+\frac{100}{100}\right)}{\left(1+\frac{100}{128.8}\right)} = 0.7881$$

The lowest amplitude at the receiver occurs when the receiver input resistance is lowest.

$$V_{AMP} = \frac{0.4\left(1+\frac{100}{100}\right)}{\left(1+\frac{100}{77.64}\right)} = 0.3497$$

6.4.6 Long Term Frequency Accuracy

There are several considerations for choosing instruments to measure long term frequency accuracy. The long term frequency accuracy of the instrument time base needs to be significantly better than the 350ppm limit in this specification; many oscilloscopes do not have this frequency accuracy. In general, equivalent time oscilloscopes cannot be used for this purpose since they require a trigger synchronous with the data.

A method to measure the long term frequency accuracy is to use a frequency counter. Many spectrum analyzers have frequency counters built in. The test setup shown in Figure 56 below shows the connections. The transmitter under test sends a HFTP (D10.2) signal to the spectrum analyzer. The signal may or may not have SSC, a 30kHz frequency modulation on it. Set the spectrum analyzer for a center frequency of 750MHz at Gen1 or 1.5GHz at Gen2, a frequency span of 100kHz (with SSC on, frequency span of 20MHz, resolution BW to 300kHz, the video BW to 300kHz), a counter resolution of 10Hz or better (350ppm at 1.5GHz is 525kHz), and place the marker on the peak signal (center of peaks with SSC on). The counter reads the long term frequency of the transmitter, the accuracy is a percentage.

When SSC is present, the measurement is a combination of the long term frequency accuracy and a frequency offset due to the SSC modulation. Measure the span of the modulation and profile. Since the counter will provide an average measurement of frequency, the profile must be considered. If the profile of the SSC modulation is not symmetrical, this must be considered when determining the actual long term frequency.

There are other instruments that contain frequency counter with a stability significantly better than 350ppm. For example some BERT equipment has a frequency counter on the clock input. There are also stand alone frequency counters.

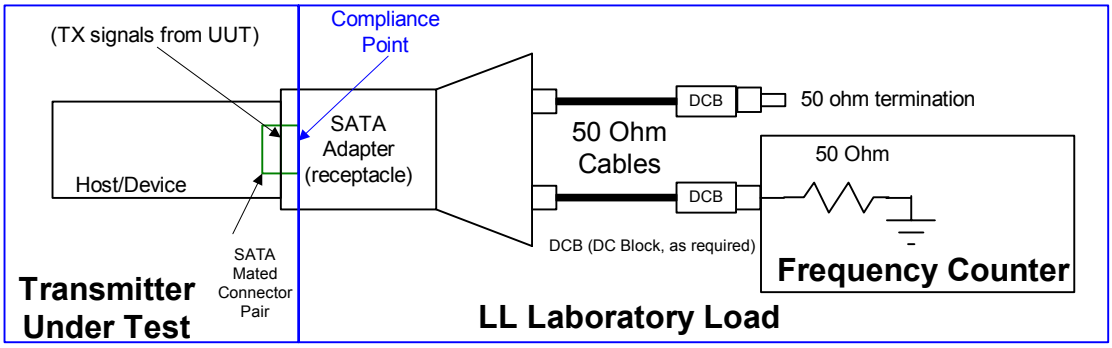


Figure 56: TX Long Term Frequency Measurement

6.4.7 Jitter Measurements

This section does not apply to Gen1i jitter measurements.

Jitter is the difference in time between a data transition and the associated Reference Clock event, taken as the ideal point for a transition. The causes of jitter are categorized into random sources (RJ) and deterministic sources (DJ). Although the total jitter (TJ) is the convolution of the probability density functions for all the independent jitter sources, this specification defines the random jitter as Gaussian and the total jitter as the deterministic jitter plus 14 times the random jitter. The TJ specifications of Table 4 and Table 6 were chosen at a targeted BER of 10^{-12}. The BERT scan method described in section 6.4.7.1 is the only method that measures the actual TJ and is used as the reference for all TJ estimation methods. The method for estimating TJ is unique to each measurement instrument.

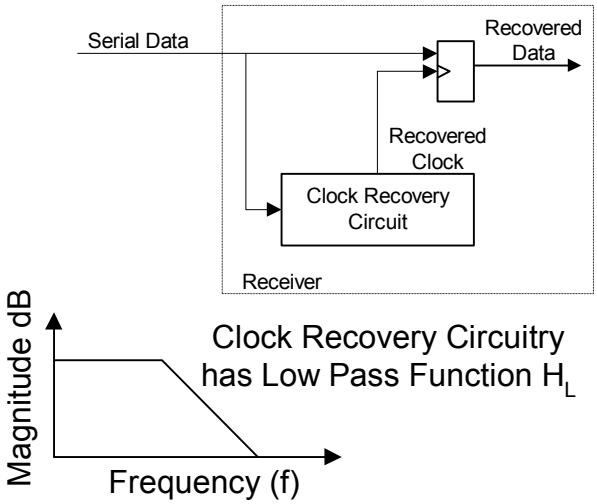


Figure 57: Receiver Model for Jitter

The jitter measurement methodology is defined as a clock to data jitter measurement. Figure 57 shows a block diagram of a deserializer input. The serial data is split into two paths. One path feeds clock recovery circuitry, which becomes the reference signal used to latch the data bits of the serial data stream. This clock recovery circuitry has a low pass transfer function H_L. The jitter seen by the receiver is the time difference of the recovered clock edge to the data edge position. This time difference function is shown in Figure 58. The resulting jitter seen by the receiver has a high pass function H_H shown in Figure 59. This defines the measurement function required by all jitter measurement methodologies. The corner frequency f_c is given is section 6.3.2.

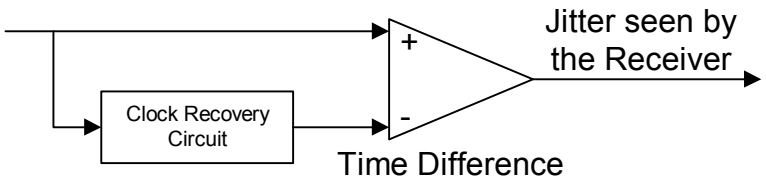


Figure 58: Jitter at Receiver

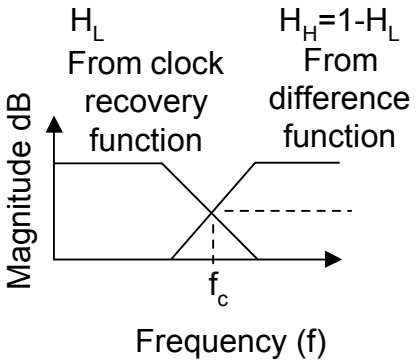


Figure 59: Jitter at Receiver, High Pass Function

This response function (green line in Figure 59: Jitter at Receiver, High Pass Function) mimics the receiver's ability to track lower frequency jitter components (wander, SSC) and not include them in the jitter measurement. This measurement methodology enables any measurement instrument to accurately measure the jitter seen by a receiver and produce measurements that correlate from measurement instrument to measurement instrument.

6.4.7.1 Jitter Measurements with a Bit Error Rate Tester (BERT)

Most instruments used to measure jitter are unable to directly measure TJ at very low bit error rates like 10^{-12} due to the time it would take to capture sufficient transitions for a statistically significant direct measurement. Instead, these instruments capture a smaller sample size and extrapolate TJ using complex, and in some cases proprietary, algorithms. The determination of TJ through extrapolation can greatly reduce the amount of time required to measure jitter but experience has shown different extrapolation-based methods can produce different results. An alternate method to measure TJ is through the use of a BERT scan method. Since a BERT scan can directly measure jitter to 10^{-12} and even lower rates in a reasonable amount of time, it also provides a means of reconciling any differences in the extrapolated value of TJ.

A BERT scan method utilizes the variable clock-to-data timing path available on a BERT. In addition to this, a PLL inside or outside the BERT that meets the requirements described in section 6.3.2 shall be used to generate the clock reference. The BERT scan systematically increases or decreases the clock-to-data timing and directly measures the BER performance at each increment of time. This is done until the time skew is found for the desired BER rate on each side of a Unit Interval. BER rates directly measured at each timing point on the left and right of a UI can be plotted to produce what is known as a bathtub curve. The time for one UI minus the time between the curves at the desired bit error rate is TJ. If those points on the bathtub curve are from directly measured data and not extrapolated, the TJ is a direct measure of TJ. Alternatively, the BERT scan is done to the left and right of the nominal zero crossing time relative to the Reference Clock to directly measure the tails of the Cumulative Distribution Function (CDF) histogram. The width of this histogram at the desired BER is TJ at that BER.

Methods do exist to extrapolate TJ on a BERT from time scan values at higher rates. While such methods can be used to predict TJ at a desired BER, only a direct measure all the way to the desired BER shall be used when using the BERT as a jitter standard for comparison to extrapolation methods.

The standard also requires a measure of DJ for compliance testing. All measures of DJ are statistically based including the estimations of DJ from a BERT. If a BERT is being used to measure TJ, the TJ values determined by that BERT may be used to estimate the DJ. Methods of estimating DJ from BERT TJ values are described in the public domain.[4] These methods involve the measurements of TJ at different BER levels using the BERT scan.

When measuring TJ and extracting the DJ and RJ components, it is common to encounter RJ measurements which are higher than actual random jitter. This is often encountered in systems where noise from the system causes jitter that is not correlated with the Serial ATA channel activity. For example, power supply noise from a system which contaminates a transmitter's bit clock generator may cause variations in the bit clock which impact jitter directly.

When making random jitter measurements, this non-correlated DJ is often included in the result which, when multiplied by 14 may lead to non-compliance to jitter specifications. This is inappropriate since non-correlated DJ is bounded, non-Gaussian and should not be multiplied by 14. Furthermore, non-correlated DJ will be included in normal DJ measurements.

Extracting non-correlated DJ from RJ measurement lies beyond the scope of this document since it usually requires in-depth knowledge of the characteristics of the non-correlated DJ and an

[4] "Estimation of Small Probabilities by Linearization of the Tail of a Probability Distribution Function" by S.B. Weinstein, IEEE Transactions on Communications Technology, Vol. COM-19, No. 6, December 1971.

appropriate algorithm for its measurement/extraction. Consequently, it is the readers' responsibility to characterize and then extract non-correlated DJ from their RJ measurements.

6.4.8 Transmit Jitter

The transmit jitter values specified in Table 4 refer to the output signal from the unit under test (UUT) at the mated connector into a Laboratory Load (LL) (for Gen1i, Gen2i, Gen1x, and Gen2x), or from the unit under test through a Compliance Interconnect Channel (CIC) into a Laboratory Load (for Gen1x and Gen2x). The signals are not specified when attached to a system cable or backplane. All the interconnect characteristics of the transmitter, package, printed circuit board traces, and mated connector pair are included in the measured transmitter jitter. Since the SATA adapter is also included as part of the measurement, good matching and low loss in the adapter are desirable to minimize its contributions to the measured transmitter jitter.

Transmit jitter is measured with each of the specified patterns in section 6.2.4.3. The measurement of jitter is described in section 6.4.7. Transmit jitter is measured in one of the following two setups for Gen2i and both setups for Gen1x and Gen2x. For Gen1i, Gen2i, Gen1x, and Gen2x the transmitter is connected directly into the Laboratory Load (LL) shown in Figure 60. Additionally, for Gen1x and Gen2x the transmitter is connected through the Compliance Interconnect Channel (see section 6.2.7) into the Laboratory Load shown in Figure 61.

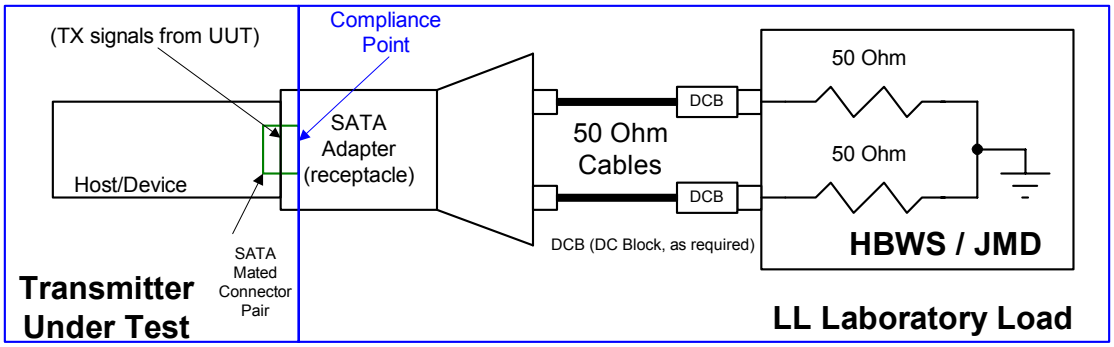


Figure 60: Transmitter Jitter Test (Gen1i, Gen2i)

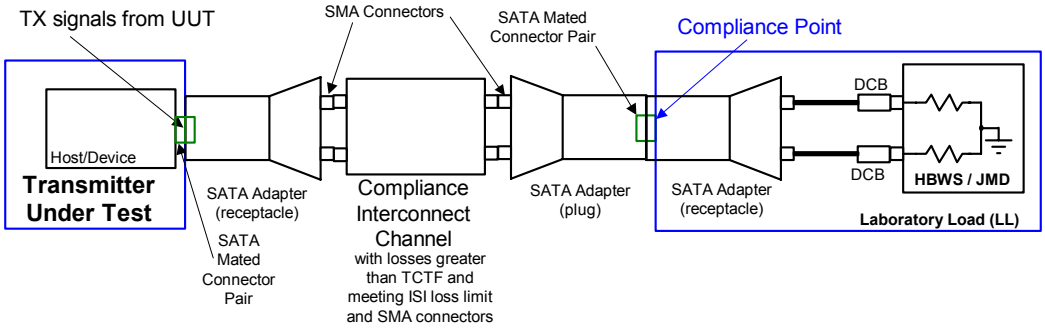


Figure 61: Transmit Jitter Test with Compliance Interconnect Channel (Gen1x, Gen2x)

Transmitter jitter is measured into the Laboratory Load (LL), or in conjunction with the Compliance Interconnect Channel; both have very good impedance matching. The jitter in an actual system will be higher since load and interconnect mismatch results in reflections and additional data dependent jitter. It is generally not possible to remove the effects of the SATA adapter on jitter since jitter due to mismatch depends on the entire test setup.

6.4.9 Receiver Tolerance

The performance measure for receiver tolerance and common mode interference rejection is the correct detection of data by the receiver. When measuring receiver and Common Mode tolerance it is necessary to set the maximum allowable jitter and common mode interference on the signal sent to the receiver and monitor data errors.

The data signal source provides a data signal with jitter, and a controlled rise/fall time with a matched output impedance. The sine wave source provides common mode interference with a matched output impedance. The two sources are combined with resistive splitters into the receiver under test (see Figure 63). Equivalent signal generation methods that provide the data with jitter, common mode interference, and an impedance matched output are allowed. All the interconnect characteristics of the receiver, mated connector pair, printed circuit board traces, and package are included in the measured receiver jitter tolerance.

Figure 62 shows a setup to set the level of jitter and common mode signal at the compliance point, on the cable side of the mated pair connector. The JMD is used as the standard for measuring jitter, and the HBWS is used as the standard for measuring the common mode interference. Since the SATA adapter is not included when setting the level of jitter, good matching and low loss in the adapter are desirable to minimize contributions to the amount of receiver jitter used in testing. Unlike other measurements, it is generally not possible to remove the effects of the SATA adapter on jitter since jitter due to mismatch depends on the entire test setup. Figure 63 shows one example approach to generate the Lab-Sourced signal.

The receiver tolerance test shall be conducted over variations in parameters SSC on and off, maximum and minimum rise and fall times, minimum and maximum amplitude, common mode interference over the specified frequency range, the test patterns LBP and the full payload COMP described in section 6.2.4.3, and jitter which includes random and deterministic jitter of various types: data dependent, periodic, duty cycle distortion. The receiver tolerance to the impairments is required over all signal variations.

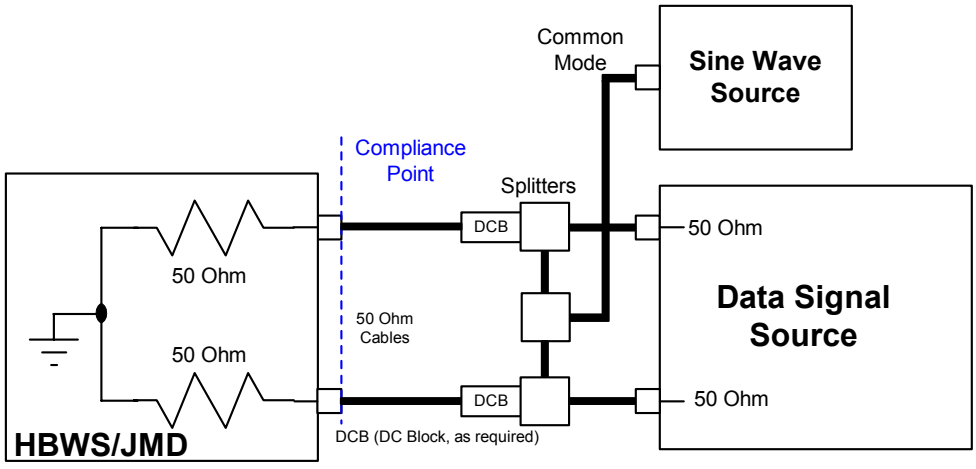


Figure 62: Receiver Jitter and CM Tolerance Test--Setting Levels

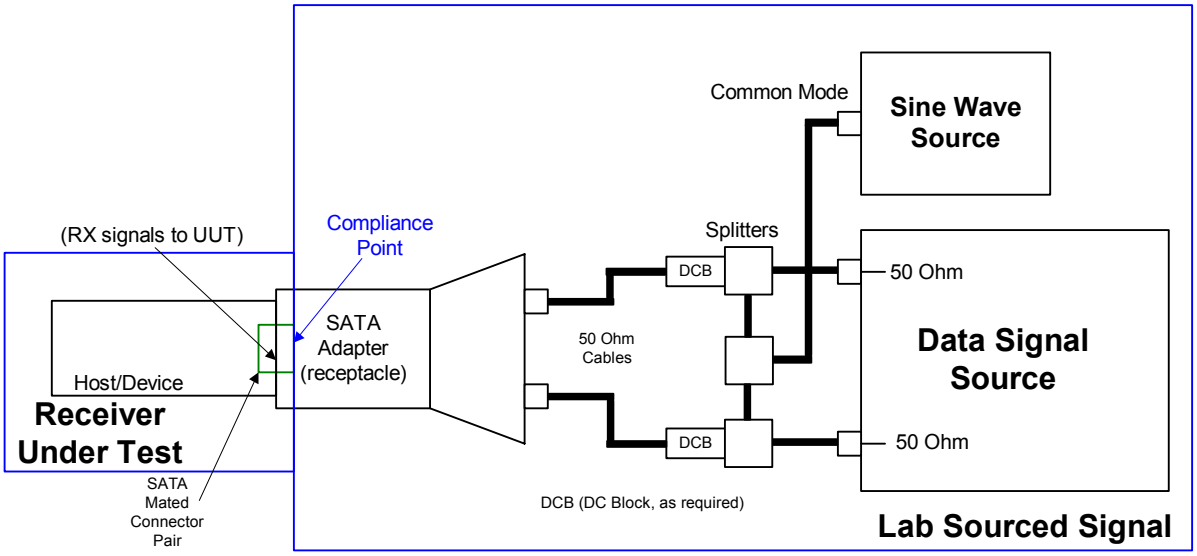


Figure 63: Receiver Jitter and CM Tolerance Test

6.4.10 Return Loss and Impedance Balance

The purpose of the return loss and impedance balance specifications (for Gen2i) is to bound the additional data dependent jitter incurred when attaching a host/device into a system. The test setup for hosts and devices is impedance matched in both differential and common modes and has good impedance balance whereas the system environment may not. Additional data dependent jitter occurs in a system from these imperfections. The return loss of a host/device quantifies the effect on the level of reflections in the system and the impedance balance controls the conversion between differential and common modes.

The differential return loss is defined as the magnitude of the differential mode reflection given a differential mode excitation, expressed in decibels. The common mode return loss is defined as the magnitude of the common mode reflection given a common mode excitation. The impedance balance is defined as the magnitude of the differential mode reflection given a common mode excitation. Each of these contribute to additional data dependent jitter in a system beyond that in a test setup.

The differential mode signal is defined by

$$v_{dm} = v_2 - v_1$$
$$i_{dm} = i_2 - i_1$$

The common mode signal is defined by

$$v_{cm} = \frac{v_2 + v_1}{2}$$
$$i_{cm} = \frac{i_2 + i_1}{2}$$

The return loss is defined by the magnitude of the reflection coefficient

$$RL = -20\log|\rho|$$

This specification describes transmitter output impedance and receiver input impedance in terms of the magnitude of a reflection of a sine wave. In a lossless line, the return loss remains constant over position. Attenuation loss in the test setup causes the measured return loss to appear higher (better matched) than actual. Figure 64: Return Loss Test--Calibration shows a setup to compensate for the loss in the cables. The short and load are assumed standards with RF connectors, for example SMA type connectors.

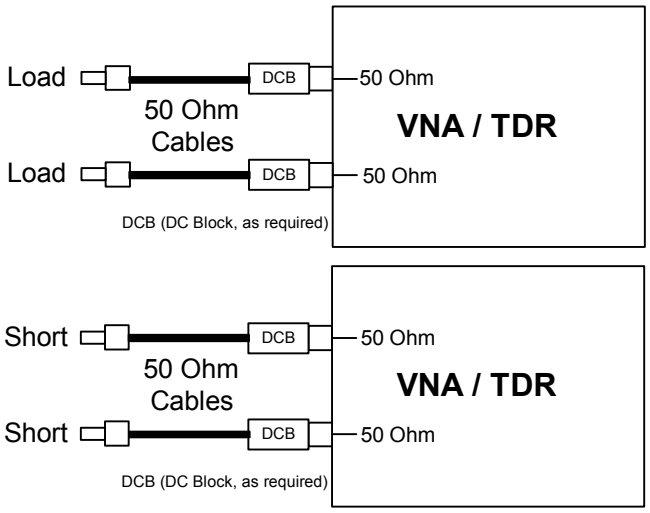


Figure 64: Return Loss Test--Calibration

A reflection test set allows the measurement of reflections in the differential mode, or in the common mode. It may consist of a TDR with processing software, a multiport vector network analyzer, hybrid couplers and directional bridges, or a 2-port vector network analyzer and processing software.
Differential return loss, common mode return loss, and impedance balance can be measured with a 2-port vector network analyzer. The VNA is connected to the host/device and the S parameters are measured (with a 50 ohm reference impedance). The differential return loss in terms of the mixed mode S parameters as well as the 2-port S parameters is given by

$$RL_{DD11} = -20\log\left|S_{DD11}\right| = -20\log\left|\frac{s_{11}+s_{22}-s_{12}-s_{21}}{2}\right|$$

The common mode return loss is given by

$$RL_{CC11} = -20\log\left|S_{CC11}\right| = -20\log\left|\frac{s_{11}+s_{22}+s_{12}+s_{21}}{2}\right|$$

The impedance balance is given by

$$RL_{DC11} = -20\log\left|S_{DC11}\right| = -20\log\left|\frac{s_{22}-s_{11}+s_{12}-s_{21}}{2}\right|$$

where the mixed mode S parameters are measured with a 4-port VNA, or alternatively the 2-port S parameters are measured with a 2-port VNA.

Figure 65: Return Loss Test shows a test setup for measuring differential return loss. Since the SATA adapter is not included, good matching and low loss in the adapter are desirable to minimize its contributions to the measured return loss. If measurements and SATA adapter are characterized with S parameters, it is possible to remove adapter and test setup effects through a deembedding process.

Test adapter imperfections affect the measurement of the unit under test; they introduce measurement uncertainty. For example, the attenuation loss in the test adapter reduces the reflection from the unit under test making the measured return loss higher than actual. An attenuation loss of 0.5dB (about 1 inch of PCB trace on FR4 at 5GHz) causes the measured return loss to

increase by 1dB over actual. The return loss of the adapter can affect the measured return loss higher or lower as the reflection from the adapter either adds or subtracts from the reflection from the unit under test. A well matched adapter with 20dB return loss can affect the measurements of a unit under test with return loss of 5dB by +-1dB. These effects are most pronounced at higher frequencies.

The measured reflection is affected by the adapter by the following measurement uncertainty equation

$$s_{11m} = \varepsilon_{00} + \varepsilon_{01}\varepsilon_{10}s_{11a} + \varepsilon_{01}\varepsilon_{10}\varepsilon_{11}\left(s_{11a}\right)^2$$

where ε_{10} and ε_{01} are the attenuation loss, ε_{00} is the input reflection, and ε_{11} is the output reflection of the adapter. s_{11m} is the measured reflection, and s_{11a} is the actual reflection from the unit under test. The return loss is related to the reflection amplitude.

For the most accurate measurements, the adapter effects can be characterized or calibrated, and then deembedded or removed from the measurements.

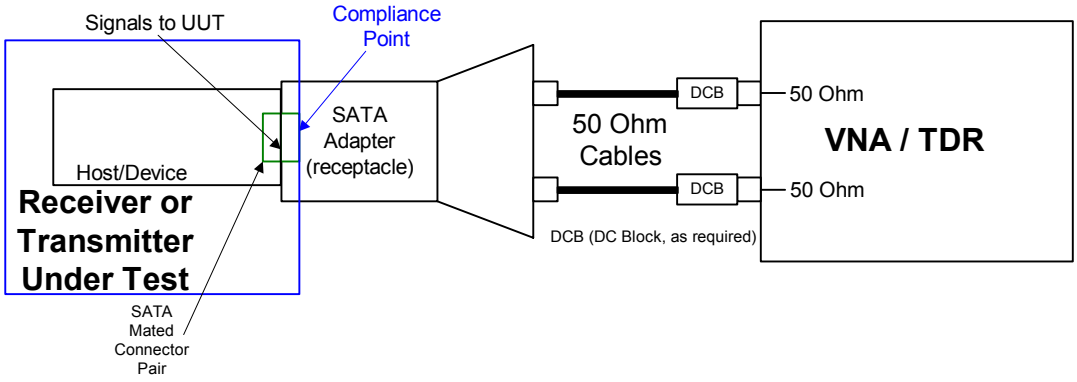


Figure 65: Return Loss Test

6.4.11 SSC Profile

Spread Spectrum Clocking is intentional low frequency modulation of the bit clock. The SSC profile is the modulation on the bit clock. To measure the SSC profile, a frequency demodulator and low pass filter are necessary. There are many possible realizations of this, in hardware and software. The low pass filter is necessary to reject undesired post-demodulation frequency components from bit patterns and jitter. To minimize these undesired signals the HFTP bit pattern shall be used. This can be produced using the BIST FIS to invoke the Transmit-Only option. The SSC Profile measurement is also used to determine the Unit Interval values.

The Reference Clock as defined in section 6.3.2 can be used with an additional low pass filter in the phase detector output to measure the SSC profile. The output is DC coupled and can be calibrated with a signal source with sufficient long term frequency accuracy.

A single shot capture oscilloscope can be used to measure the times of zero crossings (through interpolation) and perform the FM demodulator and low pass filter function. The memory record of the oscilloscope must be long enough to achieve the low pass filter cutoff frequency. The long term frequency accuracy of the oscilloscope time base should be significantly better than the 350ppm limit in this specification; oscilloscopes that do not have this frequency accuracy can be calibrated using a separate signal source of sufficient accuracy into a separate channel.

Modulation analysis tools with sufficient bandwidth provide alternative methods of measuring the SSC profile. These exist in some spectrum analyzers, modulation analyzers, or could be implemented as a separate frequency modulation receiver. Calibration is easier when the FM receiver has a DC coupled modulation path.

The low pass filter 3dB cutoff frequency shall be 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a first order low-pass of 20dB per decade.

6.4.12 Intra-pair Skew

Intra-pair skew measurements are important measurements of transmitters and receivers. For transmitters they are a measure of the symmetry of the SATA transmitter silicon (see Table 4). For receivers they are a measure of the ability to handle signal degradation due to the interconnect. At a receiver, intra-pair skew adversely affects jitter levels. In a system, intra-pair skew has a direct impact on radiated emission levels. As the measurement values are typically just a few picoseconds, care must be taken to minimize measurement error.

Figure 66 illustrates a test setup for a measurement method using a HBWS and its built-in processing. Each single-ended channel of a transmitter is measured into a Laboratory Load with DC blocks. Use HFTP and MFTP as the test patterns when measuring transmitter skew. A new displayed signal is formed by mathematically changing the polarity (arithmetic sign) and displayed with the original signal. This creates crossover points for each single ended signal, one displayed on the upper and the other on the lower part of the display. The example shown in Figure 69 of a transmitter, Ch5 and Ch6 are the two single-ended signals of the differential pair, the M5-trace is the inverted Ch5 (-Ch5), and M6 is the inverted Ch6 (-Ch6). Vertical cursors are used to measure the time between crossovers as the intra-pair skew.

Receivers shall be tested to show required performance with the RX Differential Skew set to maximum as specified in table 6. Skew can be created using test cables of differing propagation delay or active control by the data signal source within the Lab-Sourced Signal generator. Receiver skew can be setup at the same time as receiver amplitude as seen in Figure 67. Use the HFTP as the pattern when setting the skew. The skew measurement is performed as described above for the transmitter.

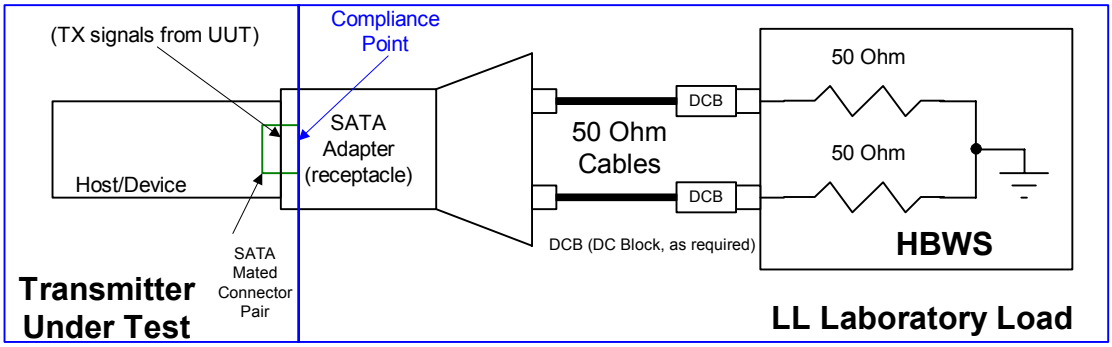


Figure 66: Intra-pair Skew test for a transmitter

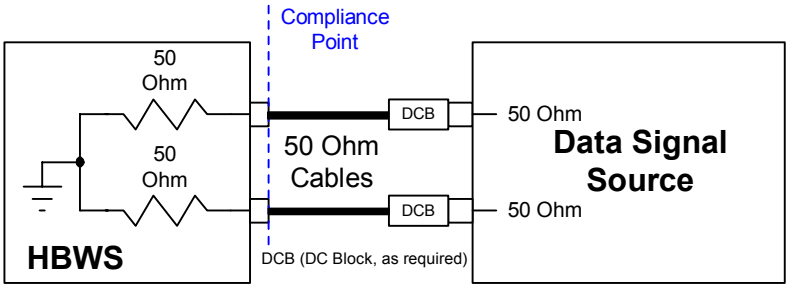


Figure 67: Receiver Intra-pair Skew Test-Setting Levels

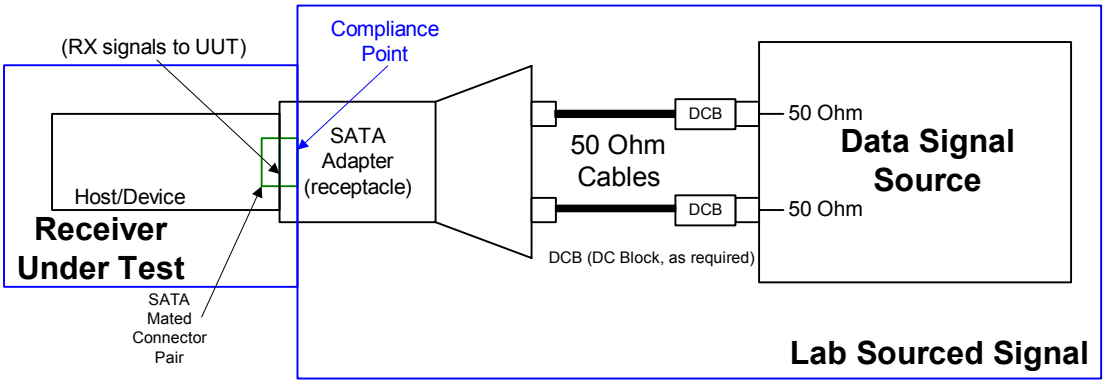


Figure 68: Receiver Intra-pair Skew Test

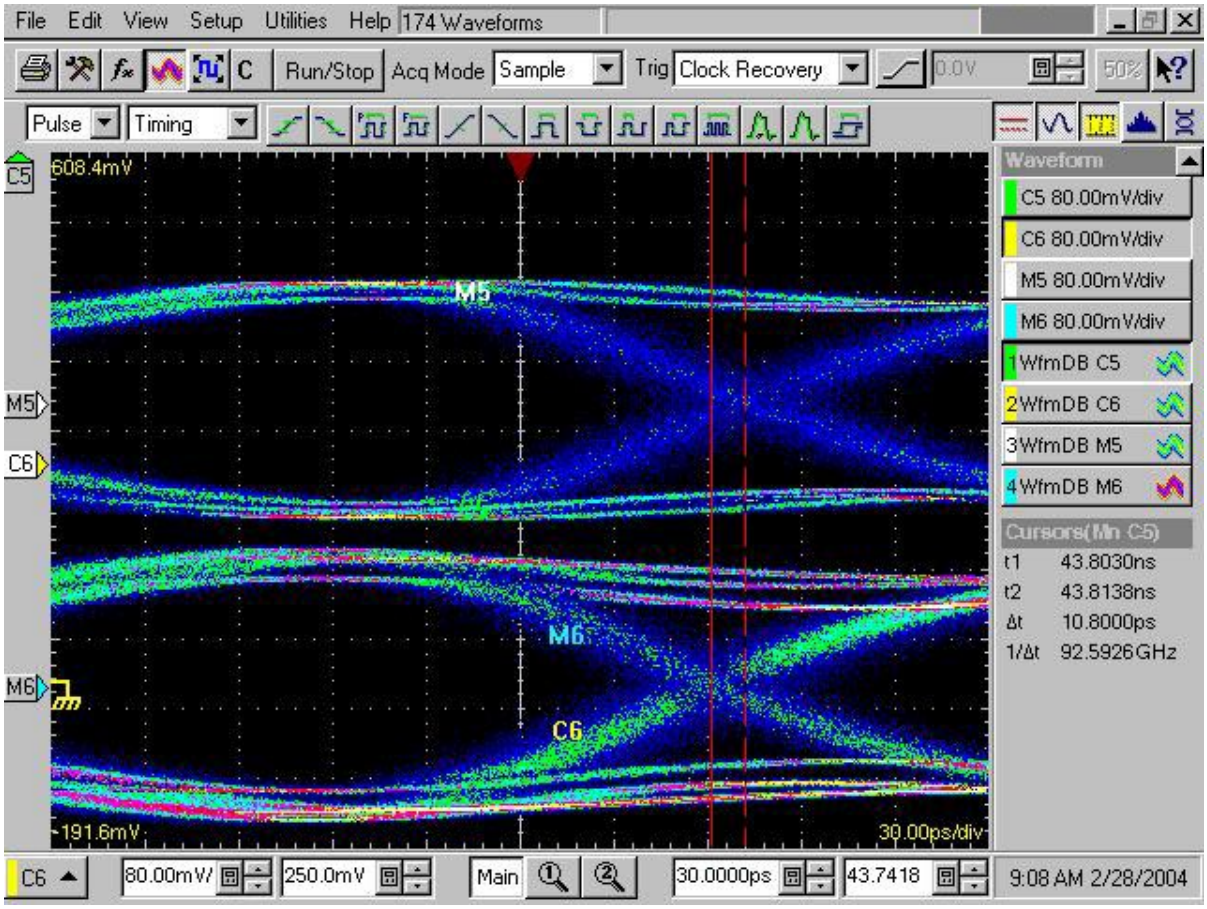


Figure 69: Example Intra-pair Skew test for Transmitter (10.8pS)

6.4.13 Sequencing Transient Voltage

Figure 70 shows the connections to the receiver or transmitter under test. Each RX or TX line is terminated to ground with a minimum impedance of 10 M Ohm that includes the probe and any external load. The value of the voltage transients during power on or power off sequencing, or power state changes seen at Vp or Vn, shall remain in the voltage range specified.

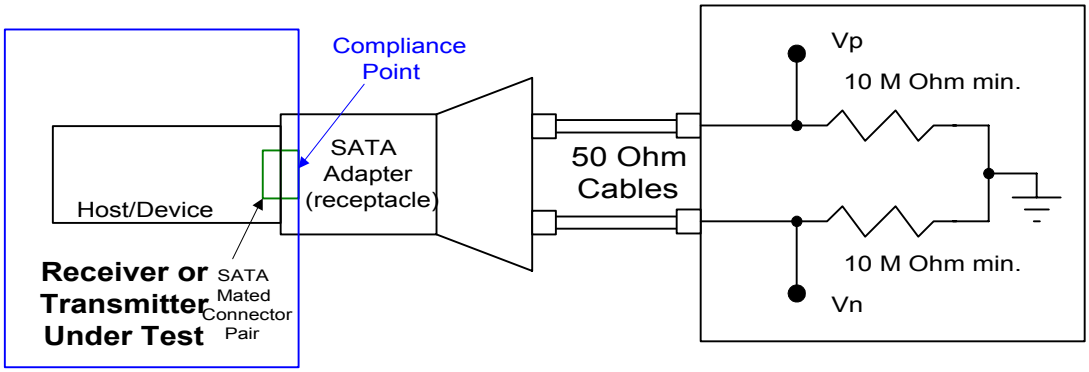


Figure 70: TX/RX Sequencing Transient Voltage Measurement

6.4.14 AC Coupling Capacitor

This measurement is only applicable to AC coupled transmitters and receivers. The AC coupling capacitor value is not directly observable at the SATA connector.

In order to measure this capacitance, each signal must be probed on both sides of the AC coupling capacitor. The unit under test is powered off and nothing is plugged into the SATA connector. In the case of coupling within the IC or where there is no access to the signals between the IC and external coupling capacitors, this parameter is not measurable as shown.

Figure 71 shows the connections to each coupling capacitor. Each coupling capacitor shall be lower than the specified maximum.

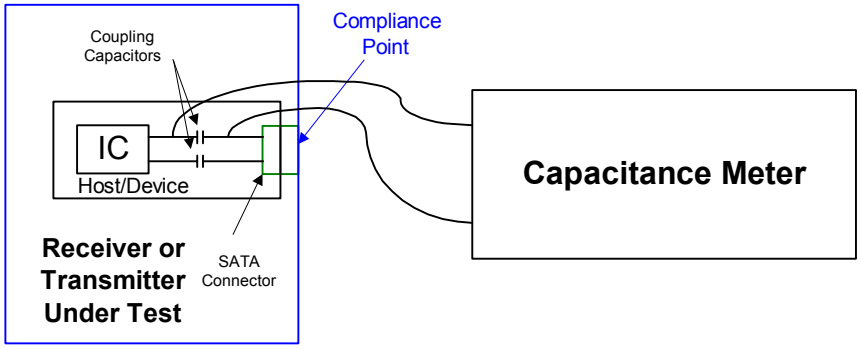


Figure 71: AC Coupled Capacitance Measurement

6.4.15 TX Amplitude Imbalance

This parameter is a measure of the match in the single-ended amplitudes of the TX+ and TX- signals. The test setup shown Figure 52 shall be used for this measurement. This parameter shall be measured and met with both the HFTP and MFTP patterns. Clock-like patterns are used here to enable the use of standard mode-based amplitude measurements for the sole purpose of determining imbalance. The measurement of differential amplitude uses a different method.

In order to determine the amplitude imbalance, single ended mode high and mode low based amplitudes of both TX+ and TX- over 10 to 20 cycles of the clock-like pattern being used shall be determined. The amplitude imbalance value for that pattern is then determined by the equation:

absolute value(TX+ amplitude - TX- amplitude)/average where average is (TX+ amplitude + TX- amplitude)/2

The amplitude imbalance value for each pattern shall be less than the maximum listed in Table 4: Transmitted Signal Requirements.

6.4.16 TX Rise/Fall Imbalance

This parameter is a measure of the match in the simultaneous single-ended rise/fall or fall/rise times of the Transmitter. The test setup shown in Figure 52 shall be used for this measurement. This parameter shall be measured and met with both the HFTP and MFTP patterns.

In order to determine the imbalance, the single ended 20-80% rise and fall times of both TX+ and TX- shall be determined for a given pattern. Two imbalance values for that pattern are then determined by the two equations:

absolute value(TX+,rise – TX-,fall)/average, where average is (TX+,rise + TX-,fall)/2
absolute value(TX+,fall – TX-,rise)/average, where average is (TX+,fall + TX-,rise)/2

Both values for each pattern shall be less than the maximum listed in Table 4: Transmitted Signal Requirements.

6.4.17 TX AC Common Mode Voltage

This parameter is a measure of common mode noise other than the CM spikes during transitions due to TX+/TX- mismatch and skews which are limited by the rise/fall mismatch and other requirements. Measurement of this parameter is achieved by transmitting through a mated connector into a Lab Load as shown in Figure 52. The transmitter shall use an MFTP (mid-frequency test pattern). The measurement instrument may be a HBWS or other instrument with analog bandwidth of at least 3 * bitrate / 2.

Separate channels must be used for TX+ and TX- and the common mode is (TX+ + TX-) / 2. This raw common mode shall be filtered with a first order filter having a cutoff equal to the bitrate / 2 to remove the noise contribution from the edge mismatches. The peak-to-peak voltage of the filter output is the AC Common Mode Voltage and shall remain below the specified limit.

6.4.18 OOB Common Mode Delta

This parameter is a measure of the offset between the common mode voltage of idle times during OOB generation and the common mode voltage during the OOB bursts. The test setup shown in Figure 52 shall be used for this measurement. A HBWS or single-shot scope may be used for this measurement, the DUT shall be configured to send an OOB sequence or multiple OOB sequences, and the instrument shall be configured so that at least 40 Gen 1 UI worth of idle time before the first OOB burst in a sequence and at least 40 Gen 1 UI worth of burst activity in the first OOB burst of a sequence are observed.

The common mode signal is (TX+ + TX-)/2 and the common mode voltage during idle for this parameter is determined by averaging the common mode voltage of a 40 Gen1 UI span of idle time within the last 60 Gen1 UIs worth of time prior to the first OOB burst in a sequence. The average common mode voltage during active time for this parameter is determined by averaging the common mode voltage of a 40 Gen1 UI span of time within the first 60 Gen1 UIs of the first burst in a sequence. The reason that the active span is taken within the first 60 Gen1 UIs of the first burst in a sequence is to minimize the affect of AC coupling RC time constant on the resulting common mode offset if one exists.

6.4.19 OOB Differential Delta

This parameter is a measure of the offset between the differential voltage of idle times during OOB generation and the average differential voltage during the OOB bursts. The test setup shown in Figure 52 shall be used for this measurement. A HBWS or single-shot scope may be used for this measurement, the DUT shall be configured to send an OOB sequence or multiple OOB sequences, and the instrument shall be configured so that at least 40 Gen 1 UI worth of idle time before the first OOB burst in a sequence and at least 40 Gen 1 UI worth of burst activity in the first OOB burst of a sequence are observed.

The differential signal is TX+ - TX- and the differential voltage during idle for this parameter is determined by averaging the differential voltage of a 40 Gen1 UI span of idle time within the last 60 Gen1 UIs worth of time prior to the first OOB burst in a sequence. The average differential voltage during active time for this parameter is determined by averaging the differential voltage of a 40 Gen1 UI span of time within the first 60 Gen1 UIs of the first burst in a sequence. The use of a span of 40 Gen1 UIs ensures that no matter what the starting time within the burst, the signal will be DC balanced and the average will represent the differential mean. The reason that the active span is taken within the first 60 Gen1 UIs of the first burst in a sequence is to minimize the affect of AC coupling RC time constant on the resulting differential offset if one exists.

6.4.20 Squelch Detector Tests

The squelch detector is an essential function in receiving OOB signaling. There are two conditions to test: when above the maximum threshold the detector shall detect, and when below the minimum threshold the detector shall not detect. Figure 72 shows the test setup to set the proper level of the OOB signal. Note the same method is used to calibrate the Lab-Sourced signal amplitude as in section 6.4.5. To ensure the proper detection, multiple tests must be done and the statistics of the results presented to show compliance.

Note: the pattern content in the OOB can affect the detection.

The timing of the gaps in the OOB bursts shall be varied to ensure compliance to the OOB timing specification (see Table 7).

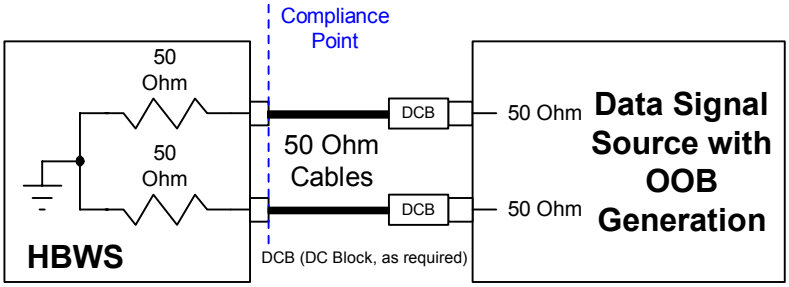


Figure 72: Squelch Detector Threshold Test--Setting Levels

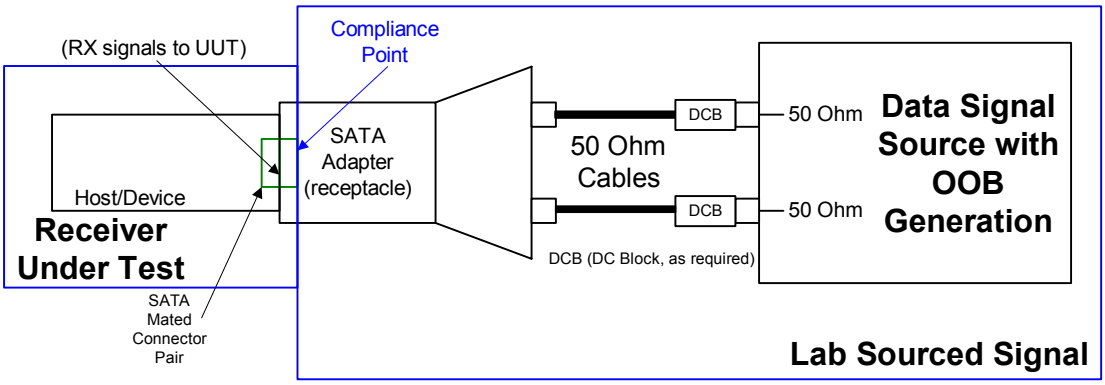


Figure 73: Squelch Detector Threshold Test

6.4.21 OOB signaling tests

Out-of-band signaling is used to signal specific actions during conditions where the receiving interface is in an active mode, a low interface power state, or a test mode.

This section specifies the set of test requirements to ensure that the OOB detector circuits will comply to the OOB signaling sequences under various conditions.

6.4.21.1 Power-on sequence

6.4.21.1.1 Calibration

When the host-controller performs impedance calibration, it shall adjust its own impedance such that the electrical requirements of section 6.2 are satisfied.

6.4.21.1.2 Speed negotiation

Speed Negotiation and transition to lower serial interface data rates shall be implemented for Gen2 compatible interfaces, negotiating and transitioning down to Gen1 speeds. There is no requirement for speed negotiation and transition to lower speeds than Gen1.

References to Gen1 and Gen2 speeds pertain to the definitions, per section 6.1.2.

6.4.21.1.3 Interface power management sequences

6.4.21.1.3.1 Partial

The interface shall detect the OOB signaling sequence "COMWAKE" and "COMRESET" when in the Partial Interface power management state.

While in the "Partial" state, the interface shall be subjected to the low-transition density bit pattern sequences of section 6.2.4.3; the interface shall remain in the Partial state until receipt of a valid COMWAKE (or COMRESET) OOB signaling sequence.

Power dissipation in this Partial state shall be measured or calculated to be less than the Phy Active State, but more than the Slumber State defined in section 6.5.4.

The requirement for a "not-to-exceed" power dissipation limit in the partial interface power management state will be classified as vendor specific, and will be documented as part of the implementation performance specifications.

6.4.21.1.3.2 Slumber

The interface shall detect the OOB signaling sequence "COMWAKE" and "COMRESET" when in the Slumber Interface power management state.

While in the "Slumber" state, the interface shall be subjected to the low-transition density bit pattern sequences of section 6.2.4.3; the interface shall remain in the Slumber state until receipt of a valid COMWAKE (or COMRESET) OOB signaling sequence.

Power dissipation in this Slumber state shall be measured or calculated to be less than the Phy Ready State, and less than the Partial State defined in section 6.5.4.

The requirement for a "not-to-exceed" power dissipation limit in the Slumber interface power management state will be classified as vendor specific, and will be documented as part of the implementation performance specifications.

6.4.22 TDR Differential Impedance (Gen1i / Gen1m)

This specification describes transmitter output impedance and receiver input impedance in terms of the peak value of a reflection given an incident step of known risetime. To achieve consistent measurements it is important to control the test conditions at the compliance point. These conditions include the signal launch (see section 6.2.6), the source match looking back into the test setup and TDR, the risetime and shape of the TDR edge, and the attenuation loss on the reflection return path to the TDR. There are various methods to control and remove the test setup effects.

Source match is a constant 100 ohms differential impedance level on the TDR trace preceding the compliance point. This can be achieved by impedance controlled test setup or a calibration procedure.

Figure 74: TDR Impedance Test--Setting Risetime shows the setup to set the risetime at the device under test. The risetime shall be set accurately at the compliance point. The shape of the TDR edge at the compliance point is affected by the edge shape of the TDR generator, the attenuation loss in the test setup, and averaging done on the received signal at the TDR.

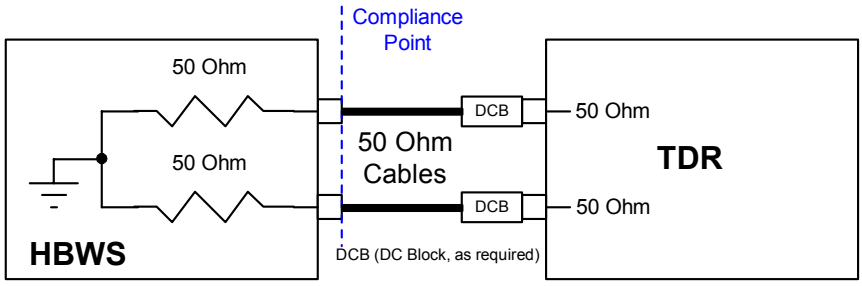


Figure 74: TDR Impedance Test--Setting Risetime

Since the SATA adapter is not included when setting risetime, good matching and low loss are necessary in the adapter to minimize errors in the measured TDR impedance.

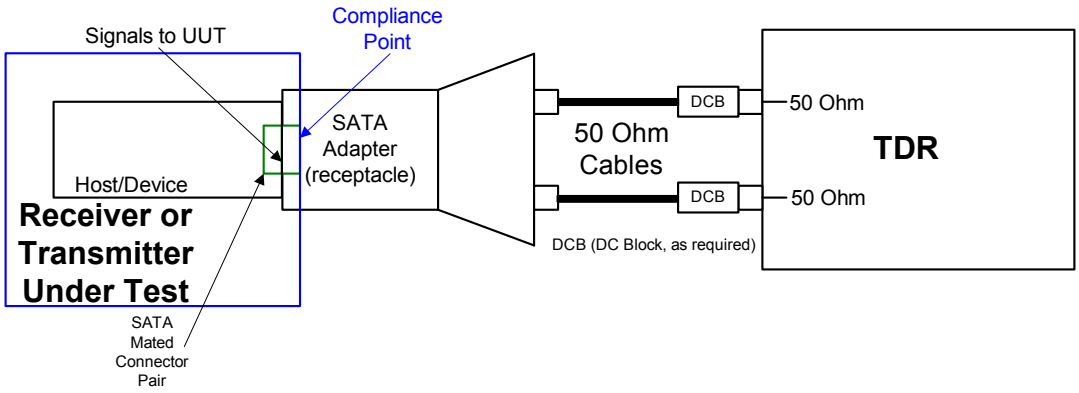


Figure 75: TDR Impedance Test

6.4.23 TDR Single Ended-Impedance (Gen1i / Gen1m)

This specification describes transmitter single-ended output impedance and receiver single-ended input impedance in terms of the peak value of a reflection given an incident step of known risetime. To achieve consistent measurements it is important to control the test conditions at the compliance point. These conditions include the signal launch (see section 6.2.6), the source match looking back into the test setup and TDR, the risetime and shape of the TDR edge, and the attenuation loss on the reflection return path to the TDR. There are various methods to control and remove the test setup effects.

Source match is a constant 50 ohms single-ended impedance level on the TDR trace preceding the compliance point. This can be achieved by impedance controlled test setup or a calibration procedure.

Figure 76 shows the setup to set the risetime at the device under test. The risetime shall be set accurately at the compliance point. The shape of the TDR edge at the compliance point is affected by the edge shape of the TDR generator, the attenuation loss in the test setup, and averaging done on the received signal at the TDR.

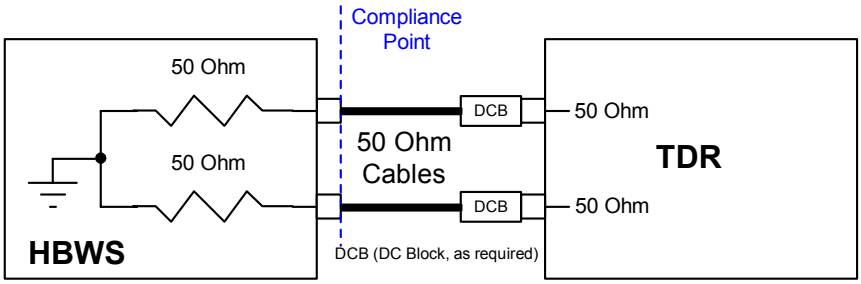


Figure 76: TDR Impedance Test--Setting Risetime

Since the SATA adapter is not included when setting risetime, good matching and low loss are necessary in the adapter to minimize errors in the measured TDR impedance.

Figure 79 shows the connections to the receiver or transmitter under test. For single-ended measurements, the TDR shall be set to produce simultaneous positive pulses on both signals of the pair. Single-ended impedance is the resulting (even mode) impedance of each signal observed independently. Both signals shall meet the single-ended impedance requirement.

6.4.24 DC Coupled Common Mode Voltage (Gen1i / Gen1m)

This measurement is only applicable to DC coupled transmitters and receivers. The following measurement on an AC coupled signal or with AC coupled probing will result in a value near or at 0V. Figure 77 shows the connections to the receiver or transmitter under test. Each RX or TX line is terminated to ground with a minimum impedance of 10 M Ohm that includes the probe and any external load. The common mode is (Vp + Vn)/2 and this term shall be in the range specified.

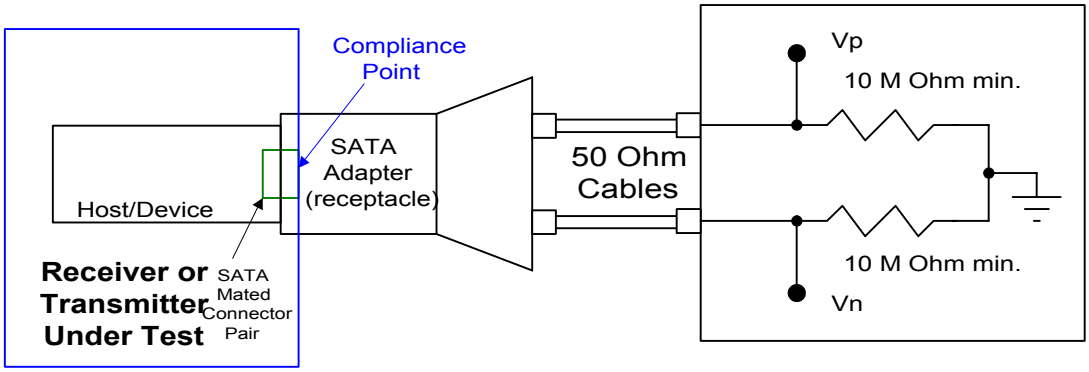


Figure 77: DC Coupled Common Mode Voltage Measurement

6.4.25 AC Coupled Common Mode Voltage (Gen1i / Gen1m)

This measurement is only applicable to AC coupled transmitters and receivers. The AC coupled common mode voltage is not directly observable at the SATA connector.

In order to measure this voltage, each RX or TX signal must be probed between the IC and AC coupling capacitor. In the case of coupling within the IC or where there is no access to the signals between the IC and external coupling capacitors, it is not measurable.

Figure 78 shows the connections to the receiver or transmitter under test. Each RX or TX line is terminated to ground with a minimum impedance of 10 M Ohm that includes the probe and any external load. The common mode is (Vp + Vn)/2 and this term shall be in the range specified.

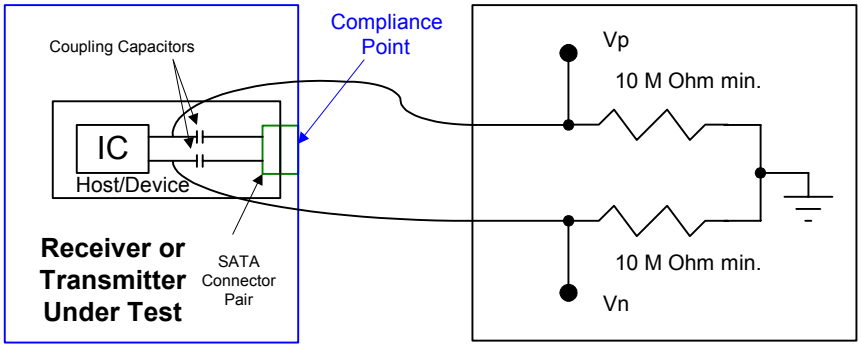


Figure 78: AC Coupled Common Mode Voltage Measurement

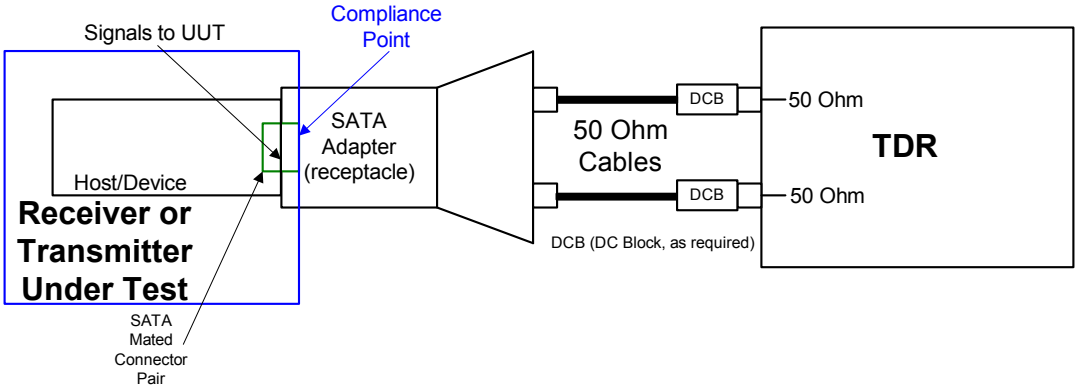


Figure 79: TDR Impedance Test

6.5 Interface States

6.5.1 Out Of Band signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy, COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of ALIGN primitives or burst of Dwords composed of 4 D24.3 characters, each burst having a duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 80 and Table 10.

The SATA Rev. 1.0a Specification allows only for the ALIGN sequence as legitimate OOB signal content, and the alternate OOB sequence defined in this section has different characteristics than the ALIGN sequence in both the time and frequency domains. The use of alternate OOB signal content may lead to backwards incompatibility with Gen1 PHYs designed in strict adherence to the SATA Rev. 1.0a Specification. Interoperability issues with Gen1 PHYs designed to the earlier SATA specification arising from the use of alternate OOB signal content are the sole responsibility of the PHY transmitting this alternate content.

During OOB signaling transmissions, the differential and common mode levels of the signal lines shall comply with the same electrical specifications as for in-band data transmission, specified in section 6.2. In Figure 80 below, COMRESET, COMINIT, and COMWAKE are shown. OOB signals are observed by detecting the temporal spacing between adjacent bursts of activity, on the differential pair. It is not required for a receiver to check the duration of an OOB burst.

In order to insure that Gen1 receivers interoperate correctly with Gen2 transmitters the OOB bursts sent by a Gen2 transmitter shall consist of Gen1 frequencies. This can be accomplished by one of two methods: (1) Transmitting the bursts at Gen1 speeds (and subsequently changing to Gen2 speeds when required during the OOB sequence) or (2) by “bit doubling” the transmitted pattern at Gen2 speed. Bit doubling involves the transmission of a bit-wise pattern created by transmitting each bit within the ALIGN or D10.2 sequence twice at the Gen2 transmission speed, thus presenting the appearance of a Gen1 pattern at the receiver. Once the bursts are sent transmission occurs at the specified transmission rate as appropriate for the speed selected.

Even though they are transmitted with apparent Gen1 timings, the OOB burst transmissions may be transmitted using Gen2 rise / fall times.

Any spacing less than or greater than the COMWAKE detector off threshold in Table 7 shall deassert the COMWAKE detector output. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (PARTIAL or SLUMBER) as described in section 6.5.4.5. The interface shall be held inactive for at least the maximum COMWAKE detector off threshold in Table 7 after the last burst to ensure far-end detector detects the deassertion properly. The device shall hold the interface inactive no more than the maximum COMWAKE detector off threshold + 2 Gen1 dwords (approximately 228.3ns) at the end of a COMWAKE to prevent susceptibility to crosstalk.

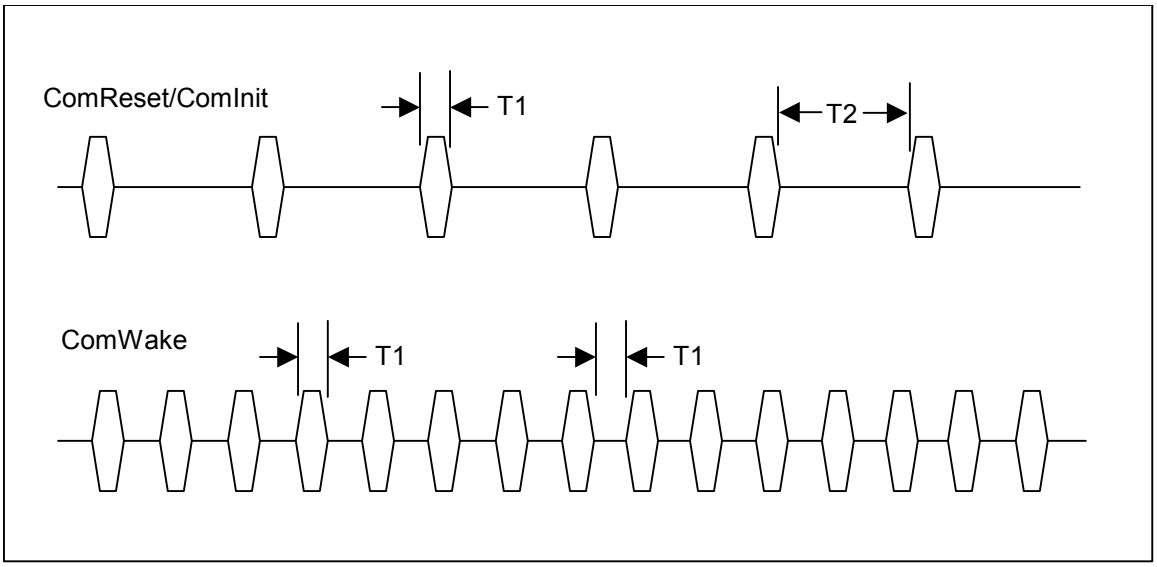


Figure 80: Out Of Band signals

Table 10: Out Of Band Signal Times

Time	Value
T1	160 UI_{oob}(106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

6.5.1.1 Idle bus status

During the idle bus condition, the differential signal diminishes to zero while the common mode level remains.

Common-mode transients, shall not exceed the maximum amplitude levels (Vcm,ac) cited in section 6.2, and shall settle to within 25 mV of Vcm,dc within Tsettle,cm, cited in section 6.2. The following figure shows several transmitter examples, and how the transition to and from the idle state may be implemented.

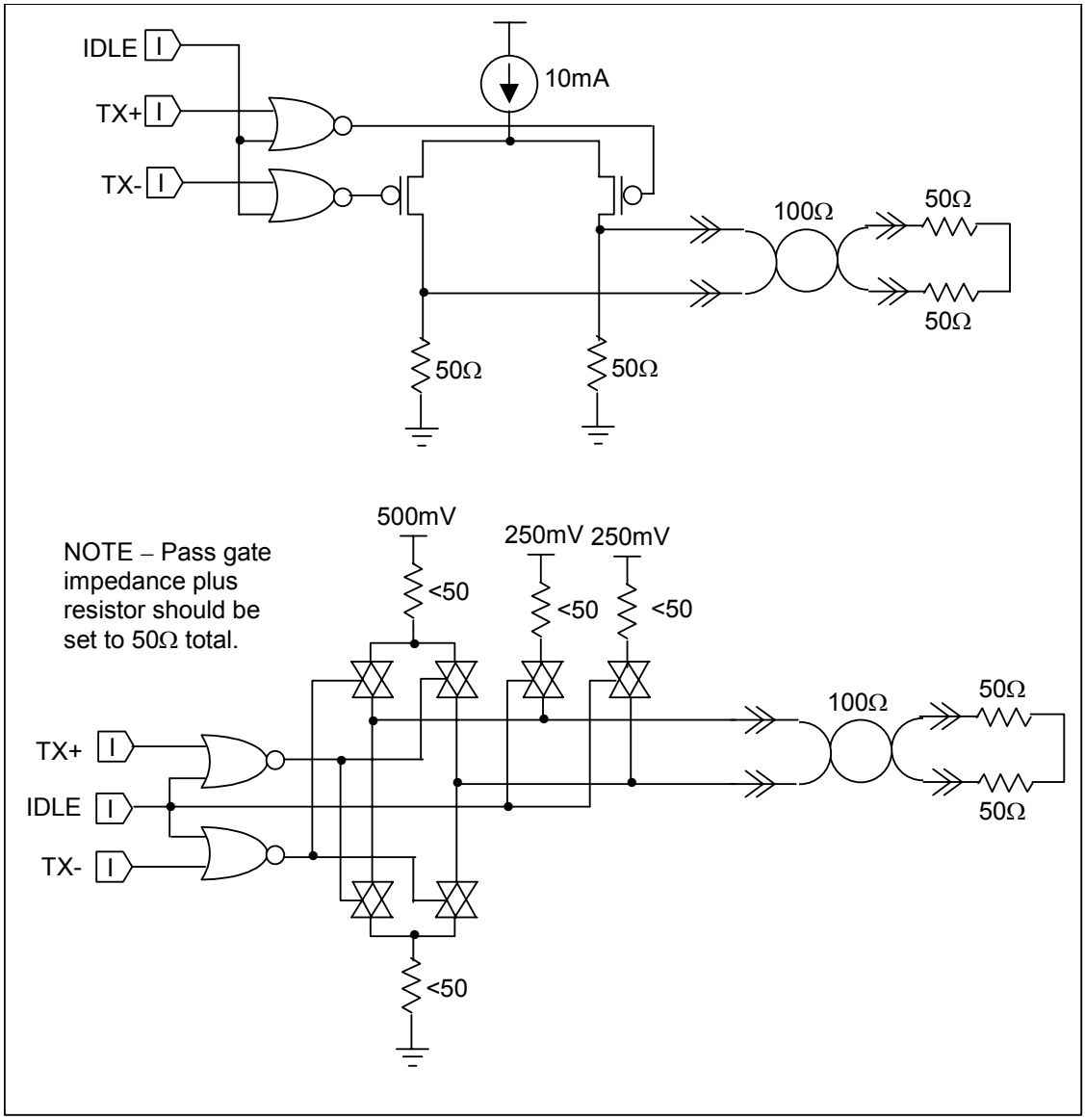


Figure 81: Transmitter examples

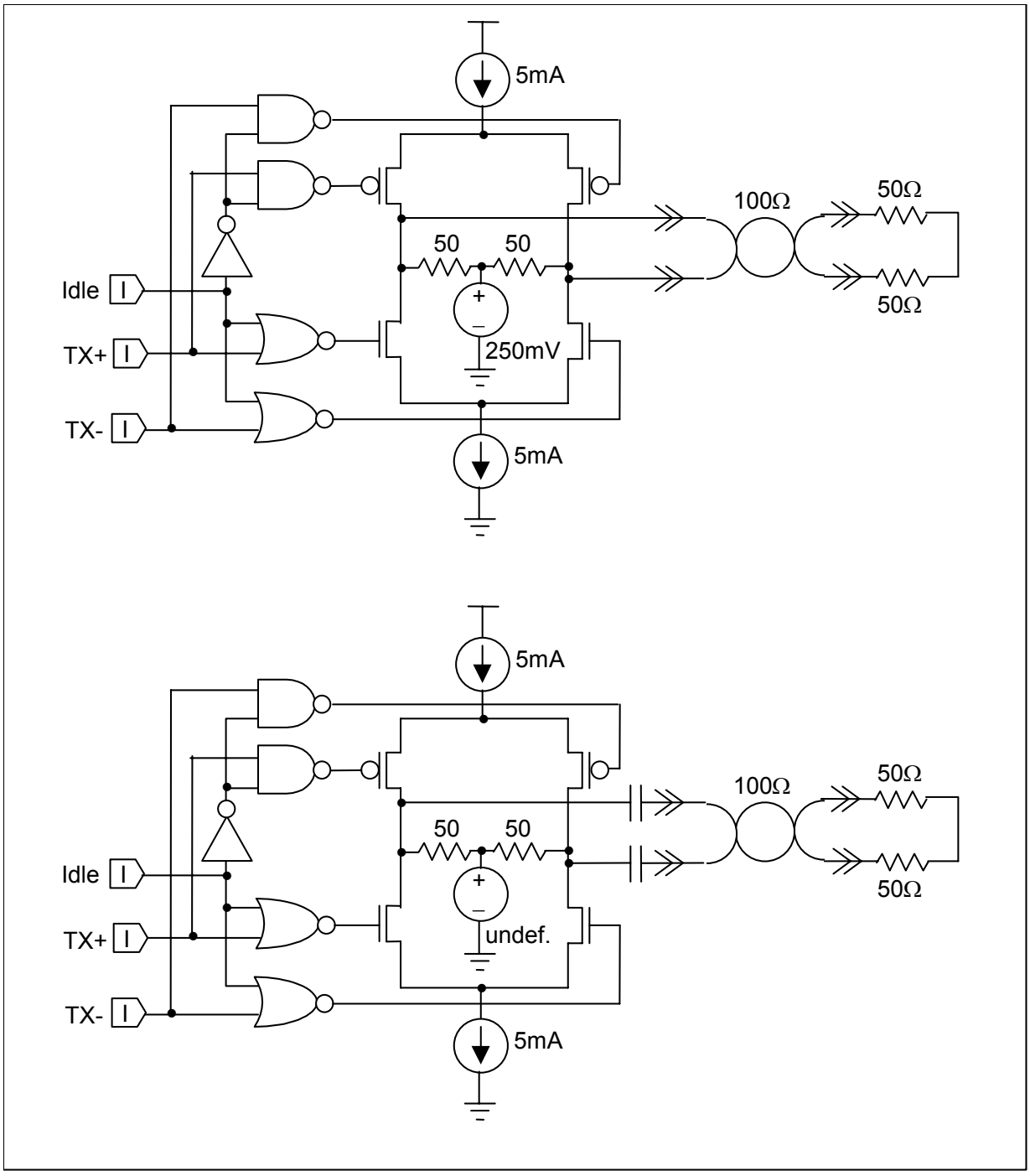


Figure 82: Transmitter examples (concluded)

6.5.1.2 COMRESET

COMRESET always originates from the host controller, and forces a hard reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition.

The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing. The COMRESET signal shall be:

1) sustained/continued uninterrupted as long as the system hard reset is asserted, or
2) started during the system hard reset and ended some time after the de-assertion of system hard reset, or
3) transmitted immediately following the de-assertion of the system hard reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hard reset signal until the COMRESET signal is transmitted.

Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector will look for four consecutive bursts with 320 ns spacing (nominal).

Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer will initiate the Reset sequence shown in Figure 83 below. The interface shall be held inactive for at least 525ns after the last burst to ensure far-end detector detects the de-assertion properly.

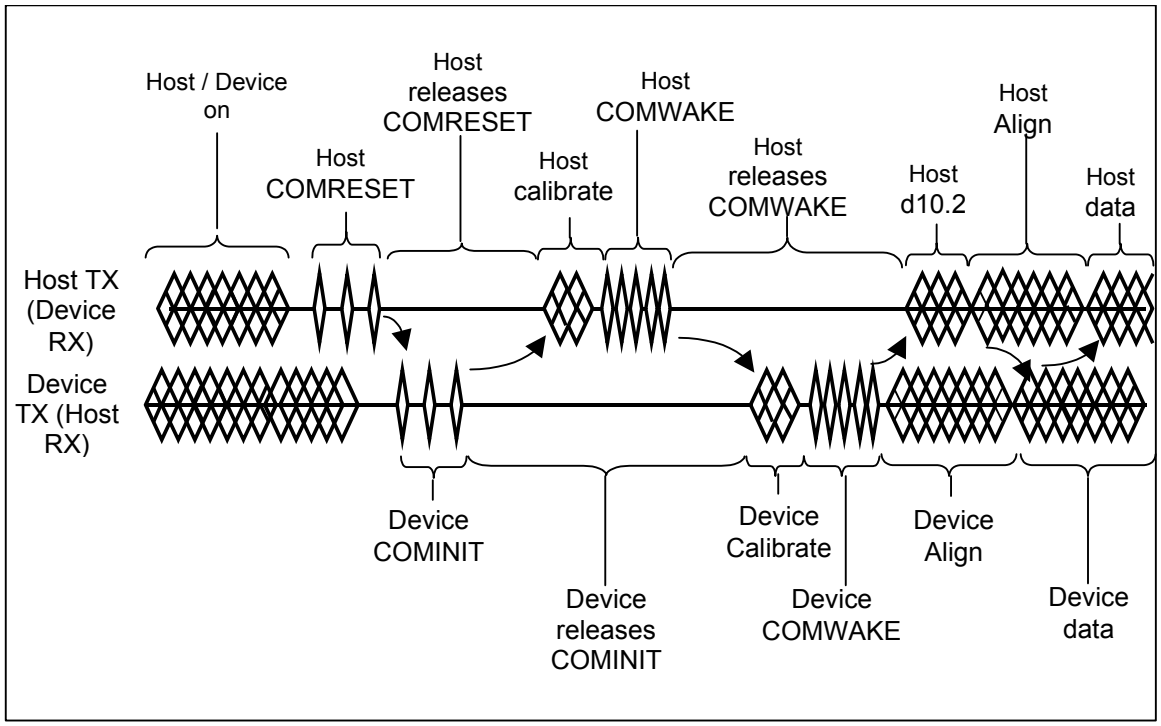


Figure 83: COMRESET sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the host causes the host to issue COMRESET
3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
5. Host calibrates and issues a COMWAKE.
6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGN Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGN primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGN Dwords at that rate for 54.6us (2048 nominal Gen1 Dword times.) This step is repeated for as many legacy speeds as are supported. Once the lowest speed has been reached without response from the host, the device will enter an error state.
7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 6.5.3) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it can acquire lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGN. This will ensure interoperability with multi-generational and synchronous designs. If no ALIGN is received within 873.8us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the application layer.
8. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNC primitive indicating it is ready to start normal operation.
9. Upon receipt of three back-to-back non-ALIGN primitives, the communication link is established and normal operation may begin.

6.5.1.3 COMINIT

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 84, below.

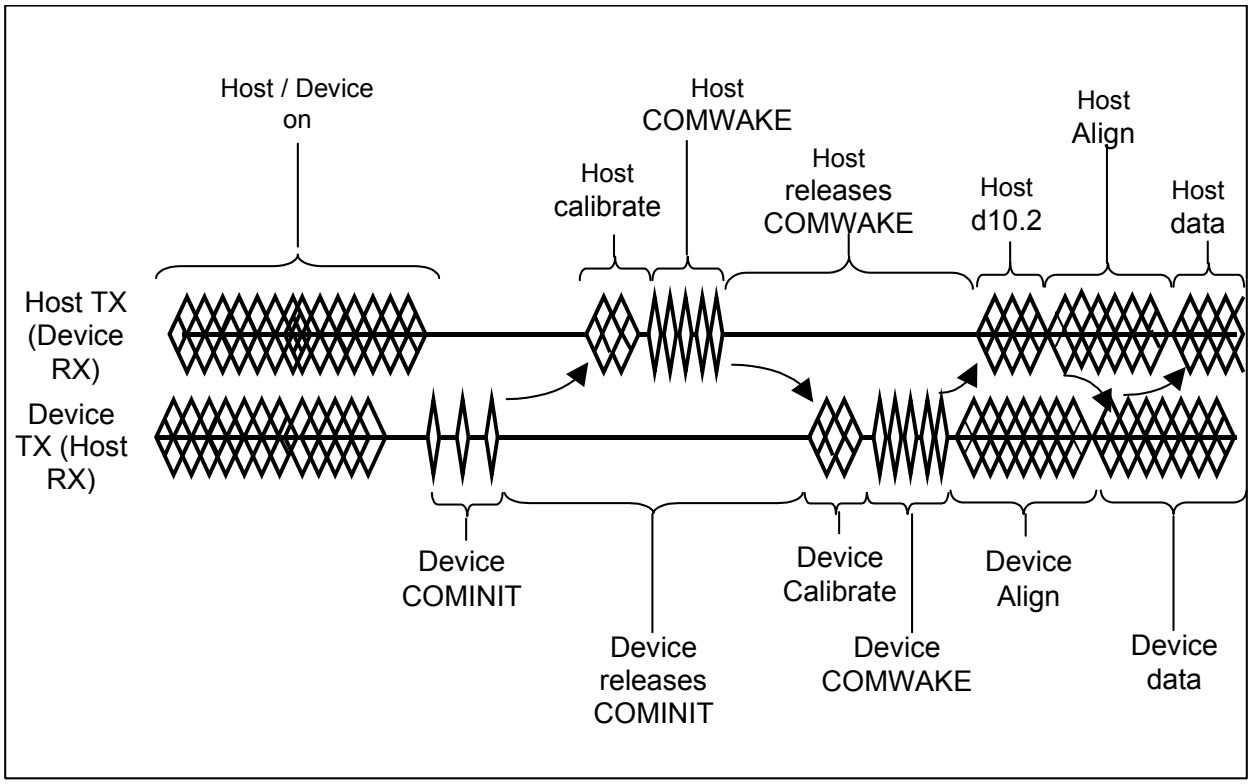


Figure 84: COMINIT sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGN Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGN primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGN Dwords at that rate for 54.6us (2048 nominal Gen1 Dword times.) This step is repeated for as many legacy speeds as are supported. Once the lowest speed has been reached without response from the host, the device will enter an error state.
5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 6.5.3) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it can acquire lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGN. This will ensure interoperability with multi-generational and synchronous designs. If no ALIGN is received within 873.8us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the application layer.
6. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNC primitive indicating it is ready to start normal operation.
7. Upon receipt of three back-to-back non-ALIGN primitives, the communication link is established and normal operation may begin.

6.5.1.4 COMWAKE

COMWAKE can originate from either the host controller or the device. It is signaled by transmitting six bursts of data separated by an idle bus condition.

The OOB COMWAKE signaling shall consist of no less than six data bursts, including inter-burst temporal spacing.

Each burst shall be 160 Gen1 UI's long and each inter-burst idle state shall be 160 Gen1 UI's long. A COMWAKE detector will look for four consecutive burst with a 106.7 ns spacing (nominal).

Any spacing less than 55 ns or greater than 175 ns shall invalidate the COMWAKE detector output. The COMWAKE OOB signaling is used to bring the Phy out of a power-down state (PARTIAL or SLUMBER) as described in section 6.5.4. The interface shall be held inactive for at least 175ns after the last burst to ensure far-end detector detects the de-assertion properly. The device may hold the interface inactive no more then 228.3ns (175ns + 2 Gen1 dwords) at the end of a COMWAKE to prevent susceptibility to crosstalk.

6.5.1.5 Design example

This section is informative and represents one possible design example for detecting COMRESET/COMINIT and COMWAKE. Other design implementations are possible as long as they adhere to the requirements listed in this specification.

The output of the squelch detector is fed into four frequency comparators. When the period is within the window determined by the RC time constants for three consecutive cycles, the appropriate signal is asserted.

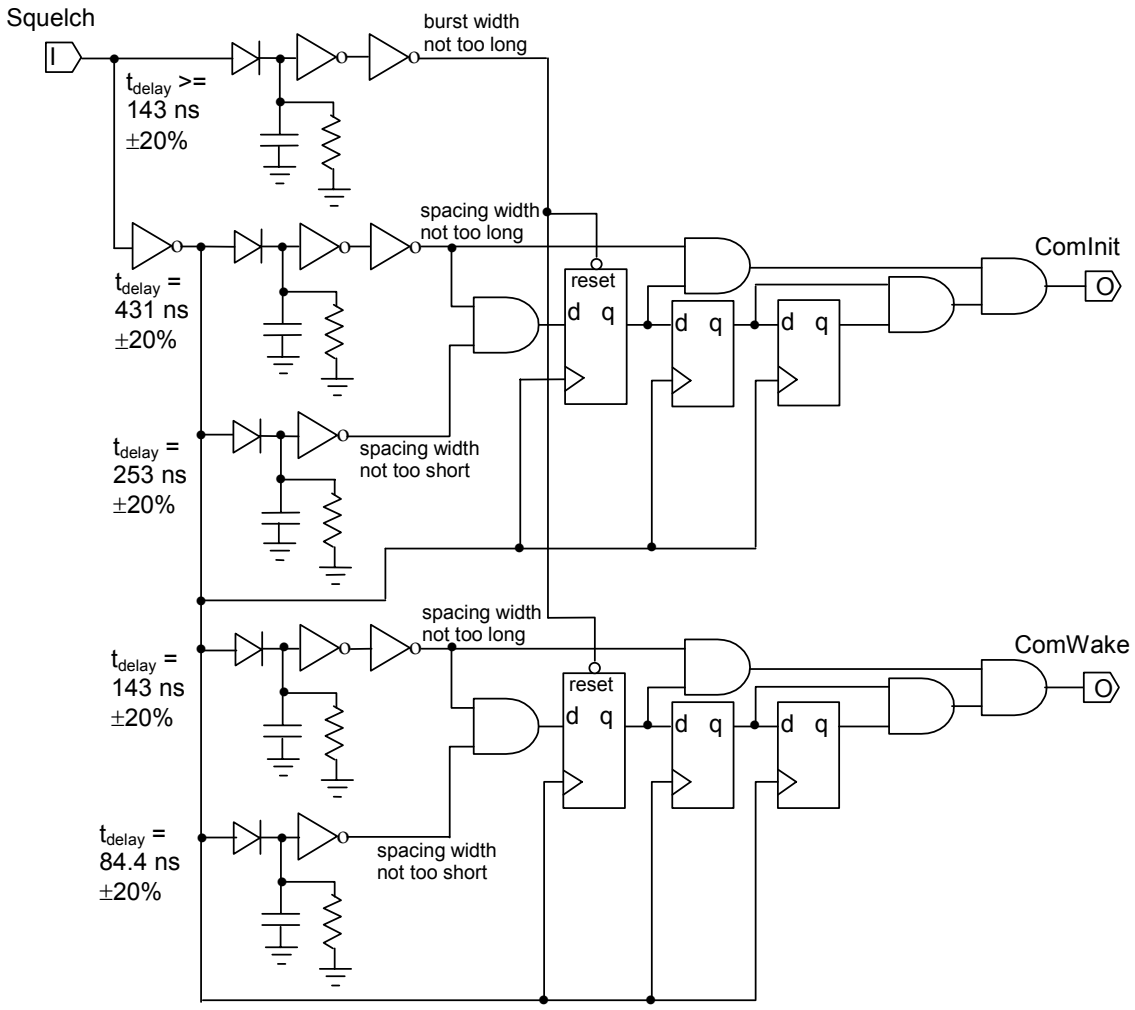


Figure 85: OOB signal detector

The Squelch detector example below makes use of a receiver with built-in hysteresis to filter out any signal not meeting the minimum amplitude. The squelch detector receiver shall be true differential to ensure common-mode noise is rejected.

The full-swing output is fed into a pulse generator that charges up the capacitor through the diode. In the absence of signal, a resistor discharges the capacitor to ground. The circuit outputs a true signal when the capacitor voltage is below the turn-on threshold of the Schmitt trigger buffer – indicating insufficient signal level. This circuit shall be enabled in all power management states and should, therefore, be implemented with a small power budget.

Figure 86, like the OOB Signal Detector figure shown in Figure 85, is intended to show functionality (informative) only, and other solutions may be used to improve power consumption as long as they comply to the electrical specifications of section 6.2, for the worst case noise environment (common-mode) conditions.

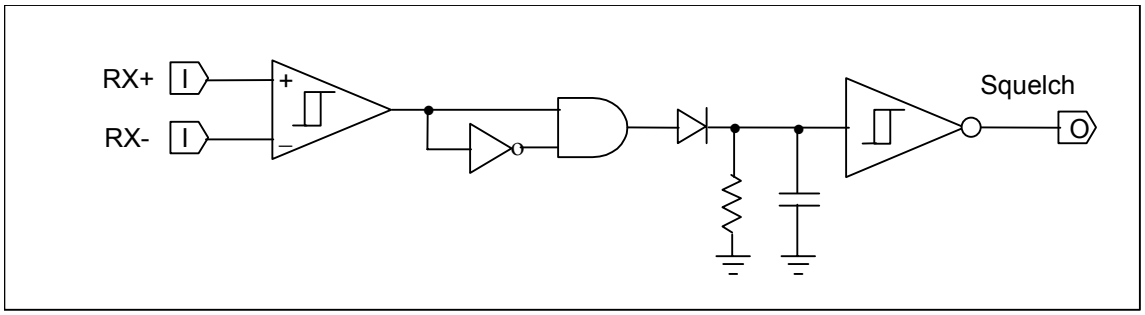


Figure 86: Squelch detector

6.5.2 Idle bus condition

During power management states (Partial and Slumber), the electrical interface shall maintain the proper common-mode levels, as cited in section 6.2, with zero differential on both signal pairs (all four conductors at 250 mV) for all interface scenarios, except for the case where both, the device and the host-controller, are AC-coupled and the conductor pairs are allowed to float.

All transmitter designs shall ensure that transition to and from the idle bus condition do not result in a disturbance in the differential baseline on the conductors. To accomplish this, an AC-coupled transmitter shall hold its outputs at zero differential with the same common-mode level as normal operation when in the partial power management mode. When operating in the slumber power management mode, the common mode level of the AC coupled transmitter is allowed to float (while maintaining zero differential) as long as it remains within the limits cited in section 6.2.

It is unacceptable to hold the TX outputs at a logical zero or one state during the idle bus condition since this will result in a baseline shift when communications are resumed.

6.5.3 Elasticity buffer management

For non-tracking implementations elasticity buffer circuitry may be required to absorb the slight differences in frequencies between the host and device. The greatest frequency difference results from a SSC compliant device talking to a non SSC device. The average frequency difference will be just over 0.25% with excursions as much as 0.5%.

The Serial ATA standard is written to support both tracking and non-tracking architectures. A non-tracking architecture shall contain the elasticity buffer within the Phy layer.

Note that since this elasticity buffer will be designed to have finite length, there needs to be a mechanism at the physical layer protocol level that allows this receiver buffer to be reset without dropping or adding any bits to the data stream. This is especially important during reception of long continuous streams of data. This physical layer protocol must not only support oversampling architectures but must also accommodate unlimited frame sizes (the frame size is limited by the CRC polynomial).

The Link Layer shall keep track of a resettable counter that rolls over at most every 1024 transmitted characters (256 Dwords). Prior to, or at the pre-roll-over point (all 1's), the Link Layer shall trigger the issuance of dual, consecutive ALIGN primitives which shall be included in the Dword count.

After communications have been established, the first and second words out of the Link Layer shall be the dual-ALIGN primitive sequence, followed by at most 254 non-ALIGN Dwords. The cycle repeats starting with another dual-consecutive ALIGN primitive sequence. The Link may issue more than one dual ALIGN primitive sequence but shall not send an unpaired ALIGN primitive (i.e. ALIGN primitives are always sent in pairs) except as noted for retimed loopback.

The ALIGN primitive consists of the following four characters

(rd+)	(rd-)	
1100000101	0011111010	Align1 (K28.5)
0101010101	0101010101	Align2 (D10.2)
0101010101	0101010101	Align3 (D10.2)
1101100011	0010011100	Align4 (D27.3)

6.5.4 Interface power states

NOTE: The Serial ATA II Extensions specification contains updates to these state machines to support optional Hot Plug and Asynchronous Signal Recovery conditions. The reader is referred to that document for the state machine specifications for optional features. However, the existing state machines in this section contain complete state machines for all required modes of behavior.

Serial ATA Interface Power States will be controlled by the device and host controller. The Serial Interface Power States shall be defined as described in Table 11: Interface Power States.

PHY READY	The PHY logic and main PLL are both on and active. The interface is synchronized and capable of receiving and sending data.
Partial	The PHY logic is powered, but is in a reduced power state. Both signal lines on the interface are at a neutral logic state (common mode voltage). The exit latency from this state shall be no longer than 10μs.
Slumber	The PHY logic is powered but is in a reduced power state. Both signal lines on the interface are at the neutral logic state (common mode voltage). The exit latency from this state shall be no longer than 10ms.

Table 11: Interface Power States

6.5.4.1 Power-on sequence state diagram

The following state diagrams specify the expected behavior of the host and device PHY from power-on to the establishment of an active communication channel.

In those states where the Phy relies on detection of received ALIGN primitives for state transitions, the Phy may rely on positive decode of the K28.5 leading character or the comma sequence (of either running disparity) as positive indication of ALIGN primitive reception rather than decoding the complete ALIGN primitive.

6.5.4.2 Host Phy Initialization state machine

As described in section 6.7.4.3, reception of a COMINIT signal shall cause the host to reinitialize communications with the device and shall unconditionally force the Host Phy state machine to transition to the HP2B:HR_AwaitNoCOMINIT state regardless of other conditions. Reception of COMINIT is effectively an additional transition into the HP2B:HR_AwaitNoCOMINIT state that appears in every Host Phy state. For the sake of brevity, this implied transition has been omitted from all the states.

HP1: HR_Reset	Transmit COMRESET[2, 3]		
	1. Power-on reset and explicit reset request deasserted	→	HR_AwaitCOMINIT
	2. Power-on reset or explicit reset request asserted	→	HR_Reset
	NOTE : 1. This state is entered asynchronously any time in response to power-on reset or an explicit reset request. 2. Shall transmit COMRESET for a minimum of 6 bursts (and a multiple of 6) 3. As described in section 6.5.1.2, COMRESET may be transmitted for the duration of this state, or it may be transmitted starting in this state and cease transmission after departure of this state, or it may be transmitted upon departure of this state.		

HP2: HR_AwaitCOMINIT	Interface quiescent		
	1. COMINIT detected from device	→	HR_AwaitNoCOMINIT
	2. COMINIT not detected from device	→	HR_AwaitCOMINIT

HP2B: HR_AwaitNoCOMINIT	Interface quiescent		
	1. COMINIT not detected from device	→	HR_Calibrate
	2. COMINIT detected from device	→	HR_AwaitNoCOMINIT
	NOTE : 1. This state is entered asynchronously any time in response to COMINIT unless during a power-on reset or an explicit reset request (in which case HP1 is entered).		

HP3: HR_Calibrate	Perform calibration[1]		
	1. Calibration complete or bypass not implemented	→	HR_COMWAKE
	2. Calibration not complete	→	HR_Calibrate
	NOTE : 1. Calibration is optional. If bypassed or not implemented, proceed directly to HR_COMWAKE.		

HP4: HR_COMWAKE	Transmit COMWAKE		
	1. COMWAKE not detected from device	→	HR_AwaitCOMWAKE
	2. COMWAKE detected from device	→	HR_AwaitNoCOMWAKE

HP5: HR_AwaitCOMWAKE	Interface quiescent		
	1. COMWAKE detected from device	→	HR_AwaitNoCOMWAKE
	2. COMWAKE not detected from device	→	HR_AwaitCOMWAKE

HP5B: HR_AwaitNoCOMWAKE	Interface quiescent	
1. COMWAKE not detected from device	→	HR_AwaitAlign
2. COMWAKE detected from device	→	HR_AwaitNoCOMWAKE

HP6: HR_AwaitAlign	Host transmits D10.2 characters at lowest supported rate[2]	
1. ALIGN detected from device (at any supported speed)[3]	→	HR_AdjustSpeed
2. ALIGN not detected from device and 880us (32768 Gen1 dwords) has elapsed since entry to HR_AwaitAlign	→	HR_Reset[1,4]
3. ALIGN not detected from device and less than 880us (32768 Gen1 dwords) has elapsed since entry to HR_AwaitAlign	→	HR_AwaitAlign

NOTE :
1. Host retries the power-on sequence indefinitely unless explicitly turned off by the application layer
2. Host shall start transmitting d10.2 characters no later than 533ns (20 Gen1 dwords) after COMWAKE is deasserted as specified in the Out Of Band signaling section
3. Host designers should be aware that the device is allowed 53.3ns (2 Gen1 dwords) after releasing COMWAKE (by holding the idle condition for more than 175ns) to start sending characters. Until this occurs, the bus will be at an idle condition and may be susceptible to crosstalk from other devices. Care must be taken so that crosstalk during this window doesn't result in a false detection of an ALIGN. For example: a compliant host may detect the de-assertion of COMWAKE in as little as 112ns, such a host should wait at least 116.3ns (175+53.3-112) after detecting the release of COMWAKE to start looking for ALIGNs.
4. The Host PHY state machine may use the transition to HR_Reset as a method of speed negotiation.

HP7: HR_SendAlign	Transmit ALIGN at speed detected	
1. Three back-to-back non-ALIGN primitives[2] detected from device	→	HR_Ready
2. Three back-to-back non-ALIGN primitives not detected from device	→	HR_SendAlign[1]

NOTE :
1. Host retries indefinitely unless explicitly turned off by the application layer
2. Non-ALIGN primitives can be detected by the presence of the k28.3 control character in the byte0 position

HP8: HR_Ready	Transmit word from Link[1]	
1. Partial signal from Link asserted	→	HR_Partial
2. Slumber signal from Link asserted	→	HR_Slumber
3. No power management request received	→	HR_Ready

NOTE :
1. PhyRdy asserted only when in the HR_Ready state and the Phy is maintaining synchronization with the incoming signal to its receiver and is transmitting a valid signal on its transmitter.

HP9: HR_Partial	Interface quiescent	
1. Partial signal from Link deasserted and no COMWAKE detected from device[1]	→	HR_COMWAKE
2. Partial signal from Link deasserted and COMWAKE detected from device[1]	→	HR_AwaitNoCOMWAKE
3. Partial signal from Link asserted	→	HR_Partial
NOTE : 1. Host Phy shall remember if COMWAKE was detected during Partial to determine if the wakeup request originated from the host or the Phy.		

HP10: HR_Slumber	Interface quiescent	
1. Slumber signal from Link deasserted and no COMWAKE detected from device[1,2]	→	HR_COMWAKE
2. Slumber signal from Link deasserted and COMWAKE detected from device[1,2]	→	HR_AwaitNoCOMWAKE
3. Slumber signal from Link asserted	→	HR_Slumber
NOTE : 1. Host Phy shall remember if COMWAKE was detected during Slumber to determine if the wakeup request originated from the host or the Phy. 2. The host Phy may take this transition only after it has recovered from slumber mode and the Phy is prepared to initiate communications. If Phy has not yet recovered from the slumber mode it shall remain in this state.		

HP11: HR_AdjustSpeed	Interface undefined but not quiescent[1]	
1 Transition to appropriate speed completed	→	HR_SendAlign
2 Transition to appropriate speed not completed	→	HR_AdjustSpeed
NOTE : 1. Some implementations may undergo a transient condition where invalid signals are transmitted during the change in their internal transmission/reception speed. The host may transmit invalid signals for a period of up to 53ns (two Gen1 dwords) during the speed transition. Transmit jitter and unit interval timing requirements may not be met during this period but shall be met for all other bits transmitted in this state. A Phase shift may occur across the speed transition time.		

6.5.4.3 Device Phy Initialization state machine

As described in section 6.7.4.2, reception of a COMRESET signal shall be treated by the device as a hard reset signal and shall unconditionally force the Device Phy state machine to transition to the DP1:DR_Reset initial state regardless of other conditions. Reception of COMRESET is effectively an additional transition into the DP1:DR_Reset state that appears in every Device Phy state. For the sake of brevity, this implied transition has been omitted from all the states.

DP1: DR_Reset[1]	Interface quiescent	
1. COMRESET not detected and power-on reset deasserted	→	DR_COMINIT
2. COMRESET detected or power-on reset asserted	→	DR_Reset
NOTE : 1. This state is entered asynchronously any time in response to power-on reset or receipt of a COMRESET signal from the host		

DP2: DR_COMINIT	Transmit COMINIT[1]	
1. Unconditional	→	DR_AwaitCOMWAKE
NOTE : 1. COMINIT transmitted for a 6 bursts duration		

DP3: DR_AwaitCOMWAKE	Interface quiescent	
1. COMWAKE detected from host	→	DR_AwaitNoCOMWAKE
2. COMWAKE not detected from host	→	DR_AwaitCOMWAKE

DP3B: DR_AwaitNoCOMWAKE	Interface quiescent	
1. COMWAKE not detected from host and part of power-on reset sequence[1]	→	DR_Calibrate
2. COMWAKE not detected from host and part of partial/slumber awake sequence[1]	→	DR_COMWAKE
3. COMWAKE detected from host	→	DR_AwaitNoCOMWAKE
NOTE : 1. Device shall remember if it was sent to partial or slumber mode for proper wakeup action.		

DP4: DR_Calibrate	Perform calibration[1]	
1. Calibration complete or bypass not implemented	→	DR_COMWAKE
2. Calibration not complete	→	DR_Calibrate
NOTE : 1. Calibration is optional. If bypassed or not implemented, proceed directly to DR_COMWAKE.		

DP5: DR_COMWAKE	Transmit COMWAKE	
1. Unconditional	→	DR_SendAlign

DP6: DR_SendAlign	Transmit ALIGN[1,2,3,5]	
1. ALIGN detected from host (device locked to incoming data)[4]	→	DR_Ready
2. ALIGN not detected from host and ALIGN primitives transmitted for 54.6us (2048[5] Gen1 ALIGN primitives) at speed other than lowest[6]	→	DR_ReduceSpeed
3. ALIGN not detected from host and ALIGN primitives transmitted for 54.6us (2048[5] Gen1 ALIGN primitives) at lowest speed[6]	→	DR_Error
4. ALIGN not detected from host and ALIGN primitives transmitted for less than 54.6us (2048 Gen1 ALIGN primitives)	→	DR_SendAlign

NOTE :
1. ALIGN should be sent at the devices fastest supported speed first
2. ALIGNS should be sent only at valid frequencies (if PLL not locked, send D10.2)
3. After COMWAKE is released as specified in the Out Of Band signaling section, the device shall ensure the interface is active (not quiescent).
4. Device designers should be aware that the host is allowed 533ns (20 Gen1 dwords) after detecting the de-assertion of COMWAKE to start sending d10.2 characters. Until this occurs, the bus will be at an idle condition and may be susceptible to crosstalk from other devices. Care must be taken so that crosstalk during this window doesn't result in a false detection of an ALIGN. Devices may extend this timeout up to an additional 54.6us (2048 Gen1 dwords) (for a max total of 109.2us), as necessary to allow their receiver time to lock to the host ALIGN.
5. Device must not leave the bus idle more than 53.3ns (2 Gen1 dwords) longer than the required 175ns to deassert COMWAKE.
6. If this is part of a device-initiated recovery from the Slumber or Partial power management state, the device Phy should resume at the speed previously negotiated and should not reduce its speed in response to failure to establish communications. Upon failing to establish communications it should instead transition directly to the DR_Error state to initiate a re-try of the ComWake sequence.

DP7: DR_Ready[1]	Transmit word from Link	
1. Partial signal from Link asserted	→	DR_Partial
2. Slumber signal from Link asserted	→	DR_Slumber
3. No power management request received	→	DR_Ready

NOTE :
1. PhyRdy asserted only when in the DR_Ready state and the Phy is maintaining synchronization with the incoming signal to its receiver and is transmitting a valid signal on its transmitter.

DP8: DR_Partial	Interface quiescent	
1. Partial signal from Link deasserted	→	DR_COMWAKE
2. Partial signal from Link deasserted and COMWAKE detected from host	→	DR_AwaitNoCOMWAKE
3. Partial signal from Link asserted	→	DR_Partial

DP9: DR_Slumber	Interface quiescent		
	1. Slumber signal from Link deasserted	→	DR_COMWAKE
	2. Slumber signal from Link deasserted and COMWAKE detected from host	→	DR_AwaitNoCOMWAKE
	3. Slumber signal from Link asserted	→	DR_Slumber

DP10: DR_ReduceSpeed	Interface quiescent		
	1. Transition to legacy (slower) speed complete	→	DR_SendAlign[1]
	2. Transition to legacy speed not complete	→	DR_ReduceSpeed
	NOTE : 1. Transition to a new speed is defined as being complete when the device is accurately transmitting a valid signal within the defined signaling tolerances for that speed.		

DP11: DR_Error	Interface quiescent		
	1. Error not due to failure to resume	→	DR_Error
	2. Resume from Slumber or Partial failed	→	DR_COMWAKE

6.5.4.4 Power-on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 6.5.4.1 comprise the normative behavior specification and is the ultimate reference.

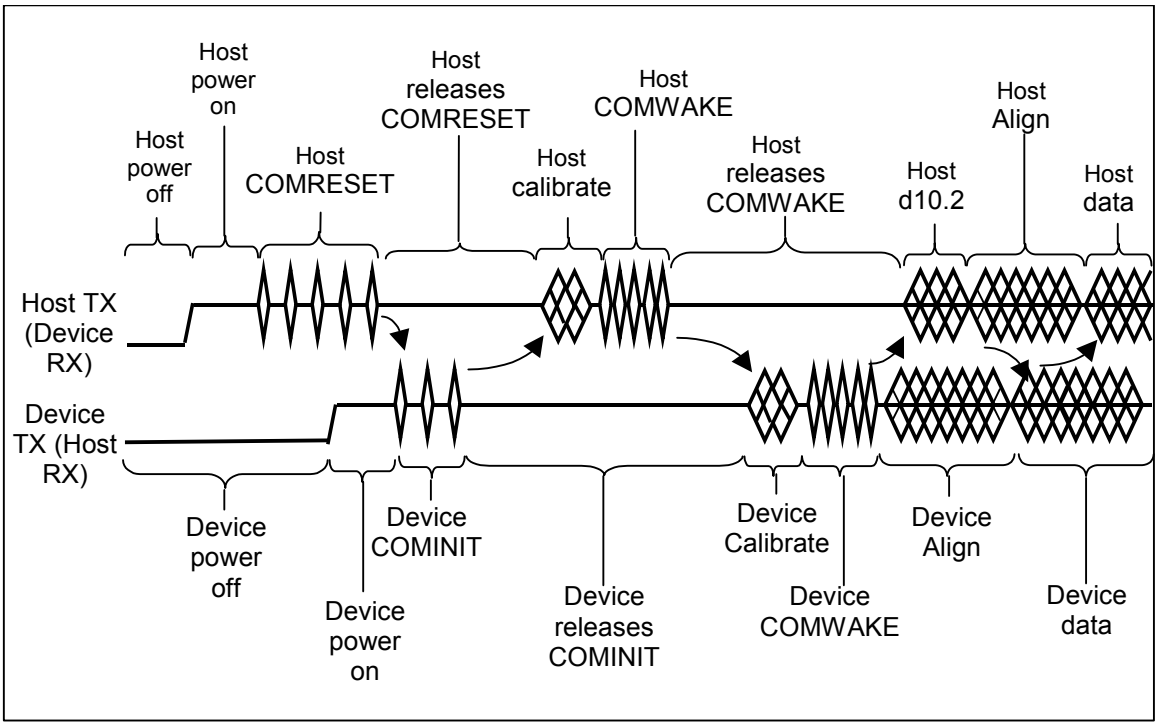


Figure 87: Power-on Sequence

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGN Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGN primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGN Dwords at that rate for 54.6us (2048 nominal Gen1 Dword times.) This step is repeated for as many legacy speeds as are supported. Once the lowest speed has been reached without response from the host, the device will enter an error state.
8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 6.5.3) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it can acquire lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGN. This will ensure interoperability with multi-generational and synchronous designs. If no ALIGN is received within 873.8us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the application layer.]
9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNC primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-ALIGN primitives, the communication link is established and normal operation may begin.

6.5.4.5 Partial/Slumber to on

6.5.4.5.1 Host initiated

The host can initiate a wakeup from the partial or slumber states by entering the power-on sequence at the “Host COMWAKE” point in the state machine. Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGNs at the speed determined at power-on.

6.5.4.5.2 Device initiated

The device can initiate a wakeup from the partial or slumber states by entering the power-on sequence at the “Device COMWAKE” point in the state machine. Calibration and speed negotiation is bypassed since it has already been performed at power-on and system performance depends on quick resume latency. The device, therefore, shall transmit ALIGNs at the speed determined at power-on.

6.5.4.6 On to Partial/Slumber

6.5.4.6.1 Host initiated

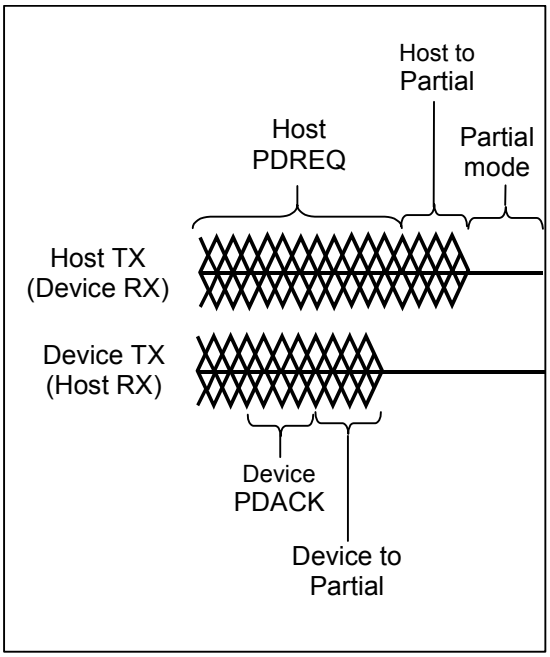


Figure 88: On to Partial/Slumber - Host initiated

6.5.4.6.1.1 Detailed sequence

1. Host Application layer sends request to host Transport layer.
2. Host Transport layer transmits request to host Link layer.
3. Host Link layer encodes request as PMREQ primitive and transmits it four times to host Phy layer.
4. Host Phy layer serializes PMREQ primitives and transmits them to device Phy layer.
5. Device Phy de-serializes PMREQ primitives and transmits them to device Link layer.
6. Device Link layer decodes PMREQ primitives and transmits request to device Transport layer.
7. Device Transport layer transmits request to device Application layer.
8. Device Application layer processes and accepts request. Issues accept to device Transport layer.
9. Device Transport layer transmits acceptance to device Link layer.
10. Device Link layer encodes acceptance as PMACK primitive and transmits it four times to device Phy layer.
11. Device Phy layer transmits four PMACK primitives to host Phy layer.
12. Device Link layer places device Phy layer in Partial/Slumber state.
13. Host Phy layer de-serializes PMACK primitives and transmits them to host Link layer.
14. Host Link layer decodes PMACK primitives and transmits acceptance to host Transport layer.
15. Host Link layer places host Phy layer in Partial/Slumber State.
16. Host Transport layer transmits acceptance to host Application layer.

6.5.4.6.2 Device initiated

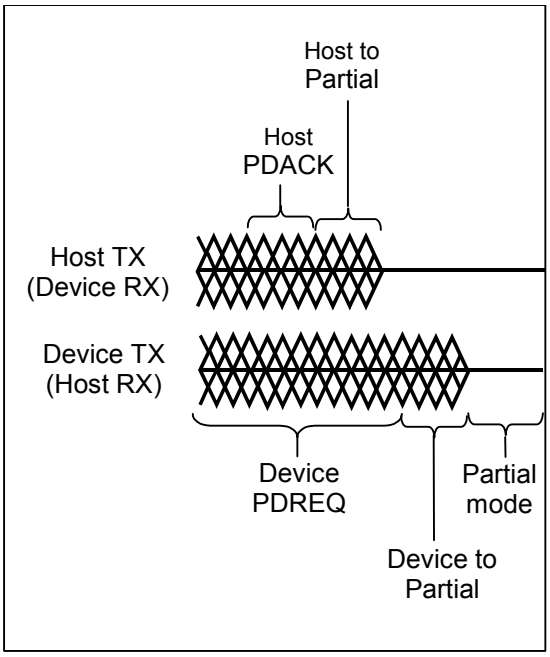


Figure 89: ON to Partial/Slumber - device initiated

6.5.4.6.2.1 Detailed sequence

1. Device Application layer sends request to device Transport layer.
2. Device Transport layer transmits request to device Link layer.
3. Device Link layer encodes request as PMREQ primitive and transmits it to device Phy layer.
4. Device Phy layer serializes PMREQ primitives and transmits them to host Phy layer.
5. Host Phy de-serializes PMREQ primitives and transmits them to host Link layer.
6. Host Link layer decodes PMREQ primitives and transmits request to host Transport layer.
7. Host Transport layer transmits request to host Application layer.
   NOTE – In this context, the host Application layer does not necessarily imply BIOS or other host CPU programming. Rather, the Application layer is the intelligent control section of the chipset logic.

8. Host Application layer processes and accepts request. Issues accept to host Transport layer.
9. Host Transport layer transmits acceptance to host Link layer.
10. Host link layer encodes acceptance as PMACK primitive and transmits it four times to host Phy layer.
11. Host Phy layer transmits four PMACK primitives to device Phy layer.
12. Host Link layer asserts Partial/Slumber signal and places host Phy layer in Partial/Slumber state.
13. Host Phy layer negates Ready signal.
14. Device Phy layer de-serializes PMACK primitives and transmits them to device Link layer.
15. Device Link layer decodes PMACK primitives and transmits acceptance to device Transport layer.
16. Device Link layer asserts Partial/Slumber signal and places device Phy layer in Partial/Slumber State.
17. Device Phy layer negates Ready signal.
18. Device Transport layer transmits acceptance to device Application layer.

6.6 Serial ATA Cable and Connector Specifications

The purpose of this section is to specify the electrical characteristics of the Serial ATA (SATA) cable and connector for Gen1i/Gen2i. The electrical characteristics defined herein will completely describe all relevant electrical behavior required to produce a working system. Details defining pin outs, mechanical descriptions, and the associated electrical specs are presented. Additionally, a test methodology is presented as a tool for characterizing SATA cables, connectors, and PCB signal paths, i.e. microstrip and stripline traces.

6.6.1 Objective

The objective of this SATA Cable and Connector section is to provide a lab engineer, marketing manager, or manufacturer a tool for testing the cable/connector environment for compliance to the SATA II specification. Inherent within this statement is the implication that the user will be provided with enough compliance information to help narrow the focus of issues related to signal integrity within the cable, host, or device.

6.6.2 Serial ATA Cable

6.6.2.1 Definition

This section does not specify a standardized SATA cable. Any cable that meets the electrical requirements described within this section is considered an acceptable SATA cable. Cable and Connector vendors have the flexibility to choose types of cable constructions and termination methods that best meet their performance and cost considerations. An example of a cable construction is given in section 6.6.2.3 for informational purpose only.

6.6.2.2 Configuration

The SATA cable consists of four conductors configured as two differential pairs. In addition to the four signal conductors, the cable may also include drain wires. The drain wires may be terminated to the ground pins in the SATA cable receptacle connectors. The conductor gauge may be within the range of 30 to 26 AWG with a maximum overall cable length of at least one meter. See Figure 90: Configuration of a Serial ATA Cable.

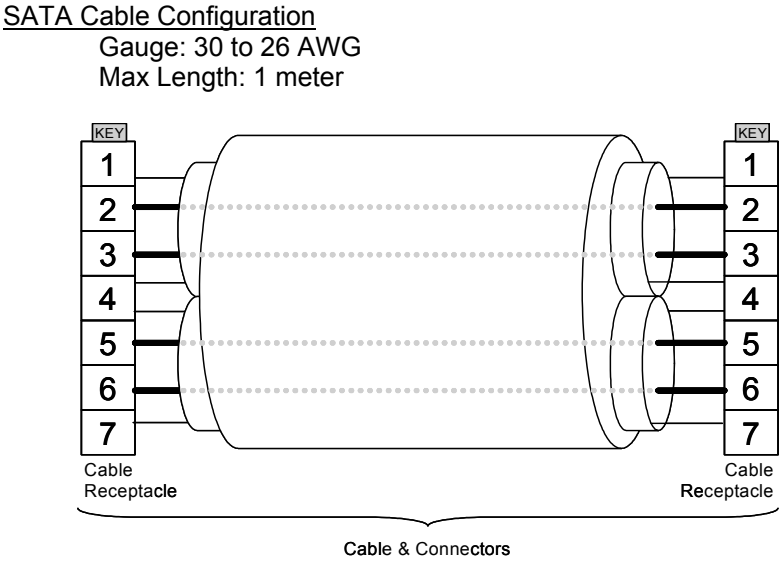


Figure 90: Configuration of a Serial ATA Cable

There are two pairs of differential signals capped with cable receptacles.

6.6.2.3 Assembly/Construction Requirements

Although construction methodologies are not specified, there ar a few essential elements of the SATA cable that must be considered. Physical characteristics of the SATA cable might include the following items. See Figure 91 for details.

- Shielded Pairs (2)
- Solid Tinned Copper (26 AWG)
- White Foam Polyolefin (43.5 mil Diameter)
- Parallel Drain Pairs (2 pr., 28 AWG – Solid Tinned Copper)
- Aluminized Polyester Foil (1 mil thick w/35mil overlap)
- Foil may be the blue longitudinal wrap that is sealed with heat
- Jacket (20 mil PVC wall)

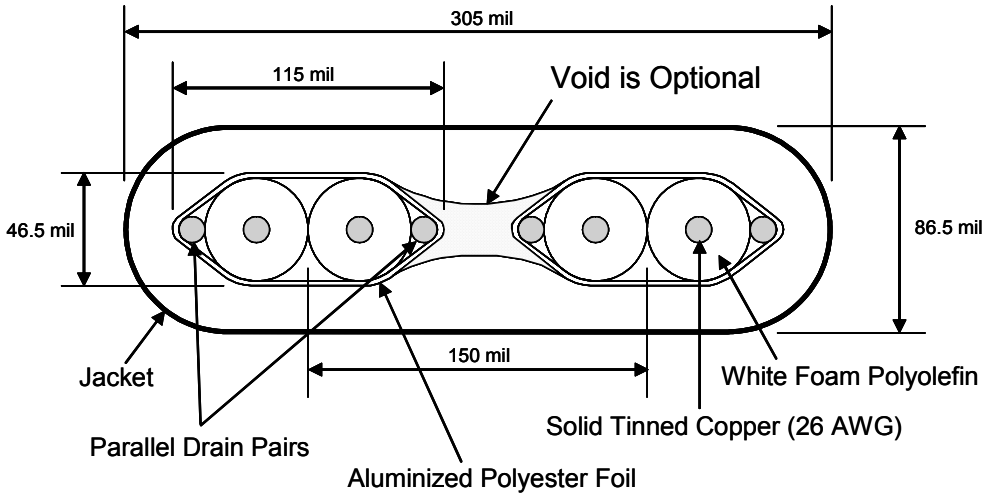


Figure 91: Detailed Cross-section of an Example Serial ATA Cable

6.6.2.4 Manufacturing Tests/Requirements

In addition to manufacturing SATA cables to meet cost and electrical constraints, it is also necessary to quantify the physical quality of the cables. Unless otherwise specified, all tests and measurements in Table 12 shall be performed within the following lab conditions:

- Cable/Connector Mated
- Temperature: 15° to 35° C
- Relative Humidity: 20% to 80%
- Atmospheric Pressure: 650 mm to 800 mm of Hg

The information in Table 12 outlines a specific group of tests that can be performed on the SATA cable to validate the quality of a cable. If an Electronic Industry Association (EIA) test is specified without a letter suffix in the test procedures, the latest approved version of that test shall be used.

Table 12: Parameters, Procedures, and Requirements for Manufacturing Tests

Parameter	Procedure	Requirements
Insulation Resistance	EIA 364-21 After 500 VDC for 1 minute, measure the insulation resistance between the adjacent contacts of mated and unmated connector assemblies.	1000 MΩ minimum
Dielectric Withstanding Voltage	EIA 364-20 (Method B) Test between adjacent contacts of mated and unmated connector assemblies.	500 VAC for 1 minute at sea level.
Low Level Contact Resistance (LLCR)	EIA 364-23 Subject mated contacts assembled in housing to 20 mV maximum open circuit at 100 mA maximum	- Initially 30 mΩ maximum. - Resistance increase 15 m Ω maximum after stress
Contact Current Rating (Power Segment)	Test Procedure • Mount the connector to a test PCB • Wire power pins P1, P2, P8, and P9 in parallel for power • Wire ground pins P4, P5, P6, P10, and P12 in parallel for return • Supply 6 A total DC current to the power pins in parallel, returning from the parallel ground pins (P4, P5, P6, P10, and P12) • Record temperature rise when thermal equilibrium is reached	1.5 A per pin minimum. The temperature rise above ambient shall not exceed 30° C at any point in the connector when contact positions are powered. The ambient condition is still air at 25° C.

6.6.2.5 Electrical Requirements

The electrical requirements for the standard internal Serial ATA cable and connector (for Gen1i/2i applications) are listed in Table 13. Additionally, the table identifies the procedure number that defines the methodology used to measure the cable and connector for the given parameter. All measurement procedures are located in Section 6.6.4.4 Test Definition / Methodology.

Table 13: Cable / Connector Measurement Parameter and Requirements

Parameter	Spec Requirement	Procedure
Mated Connector Differential Impedance	100Ω ±15%	P1
Cable Absolute Differential Impedance	100Ω ±10%	P2
Cable Pair Matching Impedance	±5Ω	P3
Common Mode Impedance	25Ω - 40Ω	P4
Maximum Insertion Loss of Cable (10-4500MHz)	6dB	P5
Maximum Crosstalk: NEXT (10-4500MHz)	26dB loss	P6
Maximum Rise Time (35ps input)	85ps	P8
Maximum Inter-Symbol Interference	50ps	P9
Maximum Intra-Pair Skew	10ps	P10

The electrical requirements for the External Single-Lane cable and connector (defined in “Serial ATA II: Cable and Connector, Volume 2”).

Table 14: External Single Lane Cable / Connector Measurement Parameter and Requirements

Parameter	Spec Requirement	Procedure
Mated Connector Differential Impedance	100Ω ±15%	P1
Cable Absolute Differential Impedance	100Ω ±10%	P2
Cable Pair Matching Impedance	±5Ω	P3
Common Mode Impedance	25Ω - 40Ω	P4
Maximum Insertion Loss of Cable (10-4500MHz)	8dB	P5
Maximum Crosstalk: NEXT (10-4500MHz)	26dB loss	P6
Maximum Rise Time (35ps input)	150ps	P8
Maximum Inter-Symbol Interference	50ps	P9
Maximum Intra-Pair Skew	20ps	P10

The electrical requirements for the External Multi-Lane cable and connector (defined in “Serial ATA II: Cable and Connector, Volume 2”).

Table 15: External Multi-Lane Cable / Connector Measurement Parameter and Requirements

Parameter	Spec Requirement	Procedure
Mated Connector Differential Impedance	100Ω ±10%	P1
Cable Absolute Differential Impedance	100Ω ±5%	P2
Cable Pair Matching Impedance	±5Ω	P3
Common Mode Impedance	25Ω - 40Ω	P4
Maximum Insertion Loss of Cable (10-4500MHz)	16dB	P5
Maximum Crosstalk: CXT (10-4500MHz)	30dB CXT	P7
Maximum Rise Time (35ps input)	150ps	P8
Maximum Inter-Symbol Interference	60ps	P9
Maximum Intra-Pair Skew	20ps	P10

Note: All External Multi-Lane signaling is at Gen1x and Gen2x levels.

6.6.3 Serial ATA Connector

There are two options when considering the SATA connector or plug. The first option is the standard TX/RX connector surrounded with ground pins while the second option includes pins that provide a power connection.

6.6.3.1 Configuration

The following two tables, Table 16 and Table 17, detail the pin names, types, and contact order of the two SATA plug options. A brief description is also included for signal, ground and power pins. With respect to the pins identified as power pins, i.e. pins P1, P2, P3 for 3.3V, pins P7, P8, P9 for 5.0V, and pins P13, P14, P15 for 12.0V, it is recommended that Serial ATA devices buss together all power delivery pins for each supply voltage.

Table 16: Simple SATA Plug

	Name	Type	Description / Mating Order
Signal Segment	S1	GND	1st Mate
	S2	A+	Differential Signal Pair A from PHY
	S3	A-	
	S4	GND	1st Mate
	S5	B-	Differential Signal Pair B from PHY
	S6	B+	
	S7	GND	1st Mate

Table 17: Power SATA Plug

	Name	Type	Description / Mating Order
Signal Segment	S1	GND	2nd Mate
	S2	A+	Differential Signal Pair A from PHY
	S3	A-	
	S4	GND	2nd Mate
	S5	B-	Differential Signal Pair B from PHY
	S6	B+	
	S7	GND	2nd Mate
Key and Spacing separate signal and power segments			
Power Segment	P1	V_{33}	3.3 V Power
	P2	V_{33}	3.3 V Power
	P3	V_{33}	3.3 V Power, Pre-charge, 2nd Mate
	P4	GND	1st Mate
	P5	GND	2nd Mate
	P6	GND	2nd Mate
	P7	V_5	5 V Power, Pre-charge, 2nd Mate
	P8	V_5	5 V Power
	P9	V_5	5 V Power
	P10	GND	2nd Mate
	P11	Reserved	Note 1
	P12	GND	1st Mate
	P13	V_{12}	12 V Power, Pre-charge, 2nd Mate
	P14	V_{12}	12 V Power
	P15	V_{12}	12 V Power
Note 1 - The pin corresponding to P11 in the backplane receptacle connector is reserved. The corresponding pin to be mated with P11 in the power cable receptacle connector shall always be grounded			

Mating Configuration Notes

- All pins are in a single row with 50 mil pitch
- If a device uses 3.3V, 5.0V, or 12.0V as a power supply, then the power pins associated with that particular supply must be bussed together, otherwise connection of the power pins is optional.

6.6.4 Serial ATA Cable/Connector Test Methodology / Signal Integrity Validation

6.6.4.1 Cable/Connector Pin Connection Definition

The following diagram in Figure 92 shows a direct cable / connector connection and highlights the signal path of the differential TX and RX pairs.

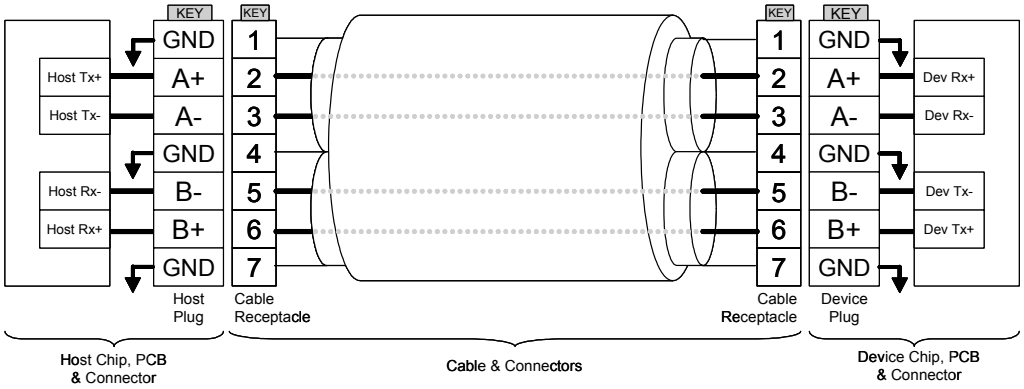


Figure 92: SATA Cable / Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

The following diagram in Figure 93 shows the connection between host and device as a direct connection. It is similar to the cable/connector connection with the exception of the cable.

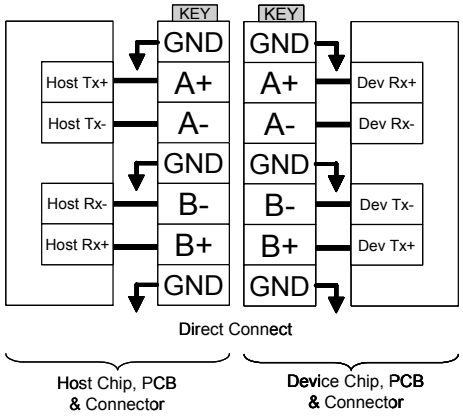


Figure 93: SATA Host / Device Connection Diagram

Notice the connection of the TX differential signal pair on the Host side to the RX differential signal pair on the Device side. A similar connection of the Host RX pair to the Device TX pair is also shown.

6.6.4.2 Test Equipment Requirements

The following list identifies the type and performance of suggested equipment to perform the characterization procedures outlined in Table 18, Table 19 and Table 20.

- High Bandwidth Sampling Oscilloscope
- TDR Module – <35ps Edge Rate Step Response
- Vector Network Analyzer – 5GHz BW
    - Suggested 4-Port or equivalent capability
- High Performance Coax Cables – ≥20GHz BW

6.6.4.3 Test Fixture Definition

Characterization of the cable/connector configuration requires an interface between the unit under test (UUT) and the test equipment and is commonly referred to as the test fixture. A primary objective in using a test fixture is to eliminate, as much as possible, the adverse signal integrity effects of the PCB. There are a couple of guidelines that should be followed when defining a test fixture. Consider the following:

- The test fixture shall consist of differential microstrip traces (100 Ohm ±5 Ohm) over a ground plane (single ended 50 Ohm ±2.5 Ohm).
- Open or shorted traces with the same length as the input signal traces shall be provided to enable the following:
    - Establish System input rise time
    - Synchronize pulses
    - Establish reference plane
- Traces for crosstalk measurements will diverge from each other.
- Provisions for attenuation reference measurement shall also be provided.

6.6.4.4 Test Definition / Methodology

Following test methodologies and making accurate measurements is crucial to both manufacturers and vendors. Purchasing decisions are based upon concrete values that are obtained from measurements. Measurements reveal the quality of a product against a specification. Because measurements are so important, it is vital that the equipment with which measurements are made is operating within acceptable tolerances. Barring any unusual phenomena, equipment that is accurately calibrated will provide the same results each time a measurement is made.

Although precaution has been used to establish an accurate and reliable test environment, there may be, at times, spurious effects that appear in the results or measurements. The spurious effects may be due to uncertainties in measurement techniques. Every effort should be made to identify the sources of such effects and correct them, if possible.

There are a number of steps within the test procedures that are similar. They are inherently used as steps of preparation in anticipation of making a measurement and are referred to as common procedures. They consist of calibration, de-skewing, establishing a reference plane, and establishing a rise time reference trace. A summary of the procedures commonly used are shown in Table 4.

Prior to performing any procedures or gathering data, ensure that the test equipment has been properly calibrated.

Table 18: Summary of Common Interconnect Measurement Procedures

Parameter	Procedure
Calibration – Follow the recommended procedure for equipment of choice.	
Procedure for Minimizing Skew between V+ and V-, Diff Signals	C1
Procedure for establishing a reference plane at the connector	C2
Procedure to establish the rise time reference trace	C3

The methodology to complete each of the common procedures is outlined in Table 19.

Table 19: Common Interconnect Measurement Procedure Methodologies

C1	**Minimizing Skew between V+ and V-, Diff Signals**
	1. Define Differential Channel Stimulus a. Channel 1/3 positive edge step response (V^+) b. Channel 2/4 negative edge step response (V^-) 2. Differential Response – Identify the differential signal (V_{diff}) as a scope response, e.g. Use math function to obtain $V_{diff} = V^+ - V^-$ (CH1-CH2 or CH3-CH4) 3. Minimize skew between the V+ (positive) and V- (negative) edges by adjusting either the V+ (CH1/3) or V- (CH2/4) edge forward or backward in time until both edges align to within 1ps.
C2	**Establishing a reference plane at the connector**
	1. Follow calibration procedures outlined in the firmware of the oscilloscope. 2. Select the define reference plane option within the scope firmware to establish a reference plane at the input of the test fixture. 3. When establishing a new reference plane, use precision 50 Ohm loads or precision air lines that are terminated with 50 Ohm loads for the test fixture.
C3	**Establishing the rise time reference trace**
	1. Configure the TDR modules to generate a differential step impulse response and identify the differential rising edge of the trace. 2. Identify the high and low voltage values of the impulse response. 3. Identify the 20% and 80% voltage levels and verify that the rise time of the step impulse is between 25ps and 35ps. There are two methods for adjusting the step impulse response to be within the desired range: a. The system rise time is to be set via equipment filtering techniques. The filter programmed equals $\sqrt{t^2_{r(observed)} - t^2_{r(stimulus)}}$ b. Capture the measurement data and perform a post processing step to filter the captured data to the desired rise time within a waveform viewer or TDR SW application. 4. Once the correct rise time has been established, verify the rise time using the reference traces on the PCB fixture.

The test methodologies and procedures outlined in Table 20 below refer to the common procedures described in Table 19 above. The actual specification requirement values for each of these methodologies are listed in section 6.6.2.5 Electrical Requirements in Table 13: Cable / Connector Measurement Parameter and Requirement.

Table 20: Interconnect Test Methodologies / Procedures

P1	**Mated Connector Differential Impedance**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record the maximum and minimum values of the near end connector differential impedance.
P2	**Cable Absolute Differential Impedance**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record maximum and minimum cable differential impedance values in the first 500ps of cable response following any vestige of the connector response.
P3	**Cable Pair Matching**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure and record the single-ended cable impedance of each cable within a pair, e.g. Z_{L1}, Z_{L2}. 3. Measure and record the maximum and minimum cable impedance values in the first 500ps of cable response following any vestige of the connector response, e.g. $Z_{L1\text{-}max}$, $Z_{L1\text{-}min}$ and $Z_{L2\text{-}max}$, $Z_{L2\text{-}min}$. 4. The desired parameter equals $Z_{max} = Z_{L1\text{-}max} – Z_{L2\text{-}max}$ and $Z_{min} = Z_{L1\text{-}min} – Z_{L2\text{-}min}$.

P4	Common Mode Impedance
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Select the negative edge step response channel to be a positive edge step response such that both channels generate a positive edge step response. 3. Measure the even mode impedance of the first step generator. 4. Perform a math function on the waveform to divide the even mode impedance response by 2. The result is the Common Mode Impedance. 5. Make the same measurement and math calculation of the second step generator. 6. The Common Mode Impedance for each step generator shall meet the requirement.
P5	**Insertion Loss**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1 and C2. 2. Measure and store the insertion loss (IL) of the fixturing using the IL reference traces provided on the board over a frequency range of 10 to 4500MHz, e.g. $IL_{fixture}$. 3. Measure and record the IL of the sample, which includes fixturing IL, over a frequency range of 10 to 4500MHz, e.g. IL_{system}. 4. The insertion loss of the sample is calculated by $IL_{sample} = IL_{system} – IL_{fixture}$.

P6	Differential to Differential Crosstalk: NEXT
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Terminate the far ends of the reference trace with characteristic impedance loads of 50 Ohms. 3. Measure and record the system and fixturing crosstalk. It is defined as the noise floor, e.g. V_{noise}. 4. Terminate the far ends of the drive and listen lines with characteristic impedance loads of 50 Ohms. 5. Connect the source to the drive pair and the receiver to the near-end of the listen pair. 6. Measure the NEXT over a frequency range of 10 to 4500MHz, e.g. V_{NEXT}. 7. Verify that the sample crosstalk is out of the noise floor, e.g. $V_{NEXT} > V_{noise}$.

P7	Multi Lane (Multi Disturber) Differential Crosstalk: ML-CXT

1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3.

2. Terminate the far ends of the reference trace with characteristic impedance loads of 50 Ohms.

3. Measure and record the system and fixturing crosstalk. It is defined as the noise floor, e.g. V_{noise}.

4. Terminate the far ends of the drive and listen lines with characteristic impedance loads of 50 Ohms.

5. Connect the source to the drive pair and the receiver to the near-end of the listen pair.

6. Measure the CXT over a frequency range of 10 to 4500MHz, e.g. V_{CXT}.

7. Verify that the sample crosstalk is out of the noise floor, e.g. $V_{CXT} > V_{noise}$.

8. $$MLCXT(f) = -20 \times \log\left(\sum_{A=1}^{7^1} 10^{-V_{CXT}(f)_l/20} \right)$$

where:

MLCXT(f) is the Multi Lane Cable assembly Crosstalk at frequency f observed on any given receive lane.

V_{CXT} (f)A is the relative crosstalk at frequency f between the receiver/victim and any combination of aggressor A[1], which exhibits less than 40dB of isolation.

f is the frequency ranging from 10MHz to 4.5GHz

A is the 1,2 –7 (receiver/victim to aggressor[1] pair combinations)

1. Aggressor: Any lane identified as a Tx (input) must be considered as a potential aggressor. This includes near end and far end Tx lane

note:

MLCXT summation calculations will account for any aggressor[1] relative to a receiver/victim pair which exhibit less than 40dB of isolation.

P8	**Differential Rise Time**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Connect the TDR step impulse response generators to the near end of the signal path under test. 3. Record the output rise time at the far end of the signal path under test.
P9	**Inter-Symbol Interference**
	1. Observe and record the cable fixtures intrinsic RJ and DJ for this setup through a 2X cal/reference trace which should be present on all SMA to cable break-out boards. 2. Connect a differential pattern source at the input of the test fixture. Generate a lone bit pattern at 3.0Gbps through the fixture. The lone bit pattern will more accurately emphasize ISI. 3. Using a JMD, evaluate the Deterministic Jitter (DJ) introduced at the end of the cable. Bear in mind the deterministic contribution from test fixtures and stimulus systems. As incident (test system induced) DJ cannot be de-convolved from the end results, it's critical one use a high quality (low jitter) fixture and stimulus system when performing this measurement.
P10	**Intra-Pair Skew**
	1. Calibrate the instrument and system using the measurement traces, then follow common procedures C1, C2, and C3. 2. Measure the propagation delay of each single ended signal within a pair at the mid point of the voltage swing, e.g. t_{delay} = V_{mid+} - V_{mid-} where $V_{mid} = \frac{V_{high} - V_{low}}{2}$.